

# Operational Amplifier Design

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E151 – Analog Circuit Design

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In this video series we're going to put together our first operational amplifier. Woohoo! We've been aiming at this for a long time, so buckle up for some exciting circuits. We'll also look at the properties that we use to describe op-amps, and at a non-linear behavior called slewing that is common in op-amps.

# Op-Amps: The Big Picture

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In this video we're going to build up the pieces of our first operational amplifier by assembling circuits that we've seen before.

## What Properties do Op-amps Need?

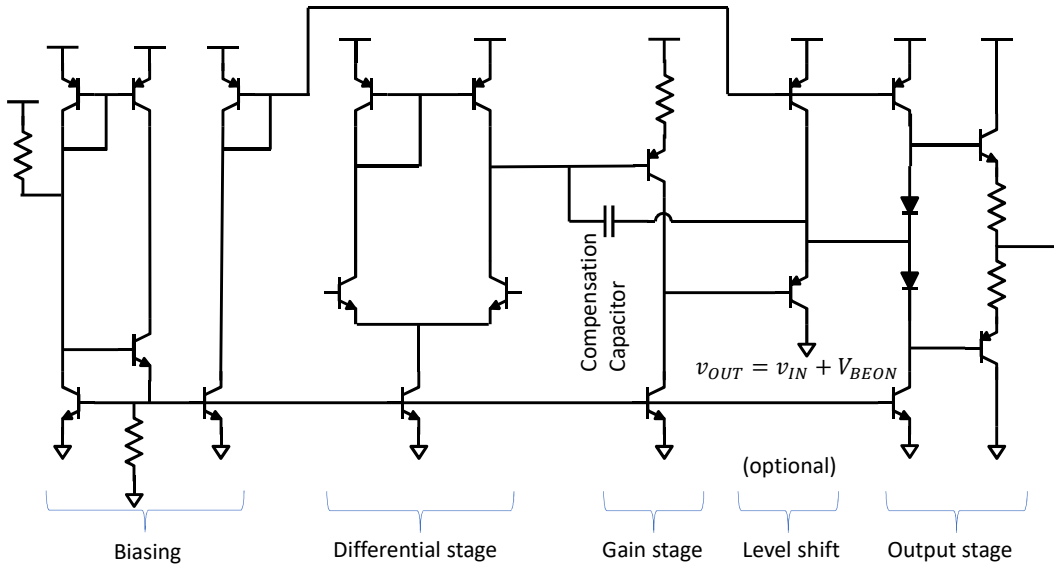
- Works at DC
- Differential inputs with infinite impedance
- Infinite gain (differential-to-single-ended)
- Zero Output Impedance

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We want to make sure that the circuit we build works like a normal op-amp, and normal op-amp operation is defined by a few important properties that describe its impedances and operation. Pause the video and try to write down a list of essential op-amp properties.

CLICK OK, there are four that I thought of: first, op-amps work at DC, which is pretty different from every amplifier we've used before now. Second op-amps have differential inputs with infinite impedance. Third, op-amps have infinite gain, and that the gain is differential to single-ended, so two inputs to one output. And finally, fourth, that the output has zero output impedance.

# Our First Op-amp Schematic (DON'T BUILD!)



So let's look at a circuit that achieves those four goals. This may look a bit big and intimidating, but it's built of pieces that we're already familiar with.

Before we start, I need to emphasize, DON'T BUILD EXACTLY THIS! I haven't simulated this, I haven't built and tested this, I haven't put numbers on any of the components on purpose to prevent people from building this. I make no guarantee that this exact schematic does anything right. However, this schematic is really good at illustrating what we're trying to do.

CLICK If we look at the left side of this circuit we see some biasing circuits. This is a self-biased VBE reference, and the resistor on the left is a big pullup that acts as the startup circuit. We have a mirror there too that creates a bias for PNP devices down the line. It's possible to just pull that PNP bias level off the mirror in the self-biased circuit, but adding this mirror decreases the static error of the mirror.

CLICK The second stage is a differential amplifier with NPN input devices and a mirror load. This provides our differential inputs (which don't have terribly high impedance in this implementation), and a bunch of gain.

CLICK Our next stage is a PNP common emitter with an active load. This stage's main job is

providing gain. Note that this stage is DC coupled to the differential stage, which is different from how we've coupled stages in the past. We have to do this because the op-amp needs to work at all frequencies, and AC coupling would ruin that behavior. (As an aside: Bypass capacitors on the emitter would also ruin that behavior, and note that we don't have one here.) However, DC coupling the stages means the large signal output voltage of the differential stage has to be just the right value to correctly bias the gain stage. We've picked a PNP input to make DC coupling easier, and I think it may be easier because the differential stage has NPN inputs, so its output is probably closer to VCC than ground. In general, you're going to have to be clever about choosing PNP vs. NPN inputs to DC couple an amplifier.

CLICK The gain stage drives into a NPN emitter follower. This is called a level shift, and it may or may not appear in an op-amp design. The main job of this stage is changing the DC output of the previous stage, in this case increasing it by one  $V_{BEON}$ , which can help DC couple your amplifier. However, if your gain stage can be safely DC coupled into your output stage, then you won't need a level shift.

Note that this is different than our usual approach: here we're using the emitter follower for its large signal effects, not its small signal effects. The large signal behavior says the output is equal to  $v_{IN}$  minus  $V_{BEON}$ , and it's cute that you can see the gain of 1 in that expression because  $v_{IN}$  and  $v_{OUT}$  have the same coefficient.

CLICK Finally, our last stage is the output stage. This stage is responsible for providing a very low output impedance for the op-amp, and also for sourcing large amounts of current in case your users decide to hook something crazy up to the output.

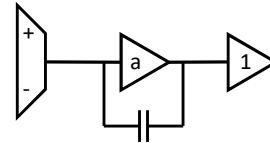
CLICK We haven't explained this capacitor, but it's called the compensation capacitor. Because it's connected across the gain stage, it's going to be Millerized. That means the dominant pole of the op-amp will be set by the compensation capacitor. Creating this very dominant pole with a compensation capacitor is a design choice, and one that can be changed in sophisticated op-amp designs. However, using a compensation cap like this is very common.

I've chosen to connect the top plate of the compensation capacitor to the differential stage output and the bottom plate to level shift output. Hooking the bottom plate to the level shift output is common even though it doesn't look exactly like Millerized caps we've seen before. Because the level shift has no small signal gain, it doesn't affect the Millerization of the cap at all, and the low output impedance of the level shift can suppresses feed-forward signals. We could have chosen to hook the bottom plate to the output of the common emitter instead, which would result in a slower dominant pole but worse feed-forward behavior.

One last note while we're thinking about capacitors: the compensation cap is the only explicit capacitor we have in the schematic. Remember that's because we can't use coupling cap or emitter bypass caps without messing up the DC behavior of the op-amp.

## Summary

- Ideal op-amps – DC operation, diff inputs, infinite  $r_{in}$  and  $a_{vd}$ , zero  $r_{out}$
- Build with three stages: differential, gain, output.
- Op-amps are DC coupled
  - No bypassing or AC coupling caps are allowed
  - Adjust the voltage at different nodes using level shifts.
  - You can also be clever about when you use NPN or PNP stages.
- Compensation cap, in feedback around the gain stage, sets dominant pole.



With Miller

# Op-Amp Design Parameters

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To evaluate the quality of an op-amp design we need some metrics that we can use. This video is going to discuss a bunch of metrics that are relevant to op-amps.

# Op-amp Design Parameters

Parameter	Symbol	Definition	Note
Which side is inverting?	$v_+/v_-$	$v_o$ up when $v_+$ up	
(Open loop voltage) Gain	$a_v$	$v_o = a_v(v_+ - v_-)$	
Differential input impedance	$r_{in,dm}$	As in a diff amplifier	Not really a diff input
Input bias current	$I_B$	As in a diff amplifier	
Input offset voltage	$v_{os}$	As in a diff amplifier	Small signal, but DC
Input common mode range	$V_{ICM}$	As in a diff amplifier	Don't care about DM range, Do care about rail-to-rail operation
Power supply rejection ratio	$PSRR$	As in a diff amplifier	Desire that it is big
Common mode rejection ratio	$CMRR$	As in a diff amplifier	Must be big for operation
Output Swing	$V_{SW}$	As in any amplifier	
Dominant Pole Location	$p_1$	As in any amplifier	Set by Compensation Cap
Slew Rate	$SR$	See next video	

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And there are a bunch of relevant parameters, so buckle up. We'll talk more about how to calculate these parameters on the next slide, I'm just getting a bunch of definitions out of the way here. These parameters can be roughly split into "new parameters for op-amps" and "parameters we've seen before", but the parameters we've seen before often have some mild twist in the op-amp context.

We'll start with "new parameters for op-amps". One really common question when you see an op-amp schematic is "which input is inverting". We denote that by adding the  $v_+$  and  $v_-$  symbols to the appropriate terminals such that the output increases when  $v_+$  increases. Another crucial measure of an amplifier is how high its gain is. I've specified that this is the "open loop voltage gain" instead of just saying gain for reasons that will be explored in future videos. The gain is multiplied by the differential input to create a the singled-ended output  $v_o$ . Since we're talking about small signal models, the small signal differential input impedance of an op-amp is important because it is how we meet the infinite input impedance specification. However, it may be surprising that this is a small signal measure at first glance. You might ask "Don't we sometimes put big voltages into an op-amp?" We do, but because op-amps are always used in feedback, and because feedback acts to minimize the difference between  $v_+$  and  $v_-$ , the inputs only ever see a small difference. That difference also isn't purely differential, but it's close enough that  $r_{indm}$  is a good proxy for input impedance seen by a source.

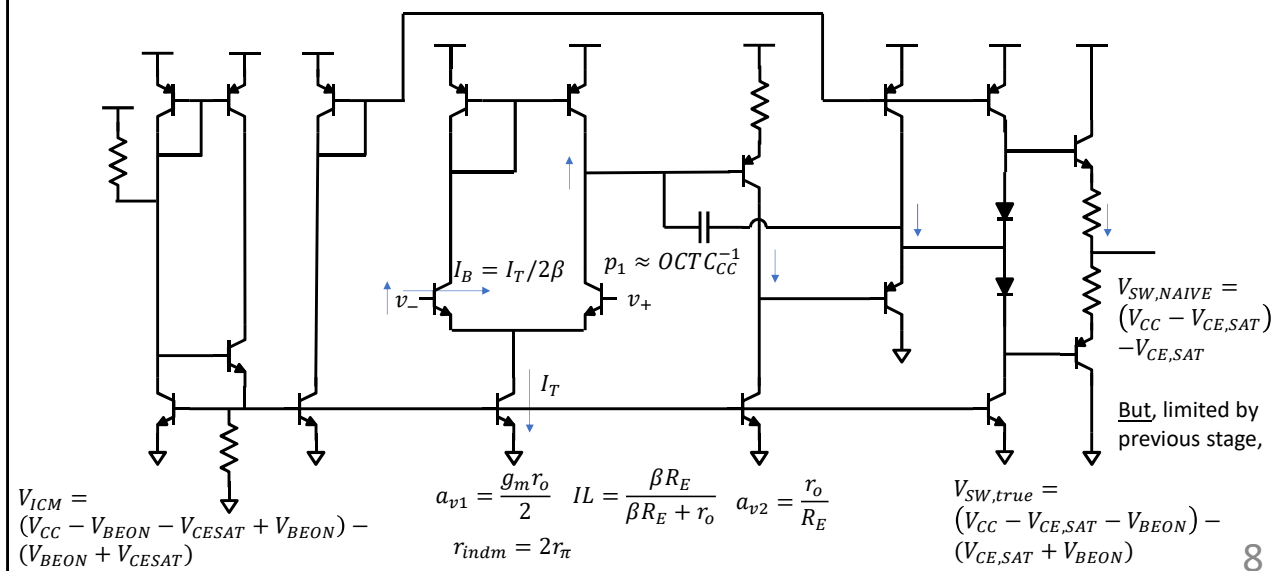


The input bias current, input offset voltage, input common mode range, power supply rejection ratio and common mode rejection ratio are all parameters that ought to be familiar from differential amplifiers. There are a few little spins on these that we care about in the context of op-amps. The input offset voltage is a small signal because offsets tend to be small, but it is a DC value. I mention this because we have often conflated the small signal approximation and the mid-band approximation in the past, but we don't need the mid-band approximation here because op-amps work down to DC. So offsets are small DC values. The input common mode range is unusually important here because op-amps are used in feedback, so the differential input is always small but the common mode varies a lot. Op-amps where the input common mode can vary from the positive to the negative supply are particularly attractive, and that condition is called a rail-to-rail input range. PSRR and CMRR matter a lot in op-amps: PSRR is important because rejection of power supply noise is always nice, and CMRR is essential because the common mode of the inputs wanders around a lot, so op-amps won't work at all without a big CMRR.

The output swing is also familiar from every amplifier we've analyzed, and it matters for the same reasons as before: it determines what signals your op-amp can provide. The dominant pole location is crucial for op-amp operation because it's related to op-amp stability. We'll talk more about stability later, but for now we want to note that calculating the dominant pole is important, and we can usually do so by finding the OCTC for the compensation capacitor.

Finally, there's a new, op-amp specific specification called the slew rate that's fancy enough to warrant its own video.

## Parameters can Be Picked Off Schematics



Now that we've gone over this list of parameters, let's see how to calculate them from a schematic. Most are pretty easy to find just by looking at the transistors!

CLICK Sorting out which input terminal is v+ and which is v- starts by perturbing one of the input terminals upwards.

CLICK We follow that effect to the output node, and note that an increase in the left terminal steers more current to the left, which will cause the left node to decrease and the right node to increase.

CLICK Decreasing the right node makes the output of this common emitter increase because more current runs through the PNP.

CLICK and that increase propagates through the level shift.

CLICK and to the output stage.

CLICK So we see that raising the left input causes the output to go up, which means that it's the non-inverting input. Note that I traced signals through in terms of node voltages here, but you can also think about currents running around the amplifier as well if that's easier to propagate. The key simplification to finding the input polarity is that you are only looking for a direction of relationship between each node or current, so you don't need to do any

math to find gains for this spec.

CLICK We find gain in much the same way we always have. The differential stage is a single-ended-to-differential actively loaded diff amp, so its gain is  $g_m \cdot r_o/2$ . Interstage loading is given by a divider between the diff stage's output resistance of  $r_o/2$  and the gain stage's input resistance of  $\beta \cdot R_E$ . Finally, the gain stage resistance is  $r_o/R_E$ . The level shift and the output stage both have a gain of 1 and a fairly high input impedance, so I'm not modeling them here.

CLICK Similarly, our differential input resistance is given by small signal parameters of our first stage:  $2 \cdot r_{pi}$  in this case.

CLICK The input bias current is given by the input device's collector current divided by  $\beta$ , and that recipe is going to be the general approach to finding input bias current. In this case, the collector current is given by the tail current over 2, but you'll need to examine your op-amp carefully to find that bias current.

CLICK The input common mode range is limited by a  $V_{OMAX}$  and a  $V_{OMIN}$ .  $V_{OMIN}$  is  $V_{BEON} + V_{CESAT}$ , and that expression comes from the input device  $V_{BEON}$  and the tail device  $V_{CESAT}$ .  $V_{OMAX}$  is  $V_{CC} - V_{BEON} - V_{CESAT} + V_{BEON}$ , and that expression comes from  $V_{BEON}$  in the mirror,  $V_{CESAT}$  of the input device and  $V_{BEON}$  of the input device.

CLICK The output swing looks like it might just be limited by  $V_{CESAT}$  of the upper and lower output device at first glance,

CLICK BUT finding output swing in amplifiers where a lot of stages have a gain of 1 can be tricky.

CLICK In this case, the swing is limited by the front half of the class AB amplifier. So we see a drop of  $V_{CESAT}$  from the current mirror devices, and then we go from base-to-emitter on the output devices to get to the output node, picking up another drop of  $V_{BEON}$ . When you're analyzing output swing, especially in an op-amp where there's only one gain stage, you need to be careful that you're not limited by a previous stage.

CLICK Finally we need to find our dominant pole. Because the compensation cap is deliberately large and deliberately in the Miller position, we can assume that the open circuit time constant of the compensation capacitor sets our dominant pole location. So find the open circuit time constant of this capacitor, and we're there. Because this is in a Miller position around a common emitter, finding this OCTC will often look like a left-right pattern, where we find the resistance seen to ground by the left and right plates. In this case, the left plate sees  $r_o/2$  from the mirror loaded emitter coupled pair in parallel with  $\beta \cdot R_E$  from the gain stage. The right plate sees  $1/g_m$  from the emitter follower. I'll leave it to you to work through the left-right pattern.

## Summary

- Op-amps have lots of parameters
- Find input polarity by perturbing one side and propagating to output
- Other params come from typical analyses, often with active loads
  - Output swing can be limited by prior stages
  - Dominant pole comes from compensation cap, usually left-right pattern

# Slew Rate

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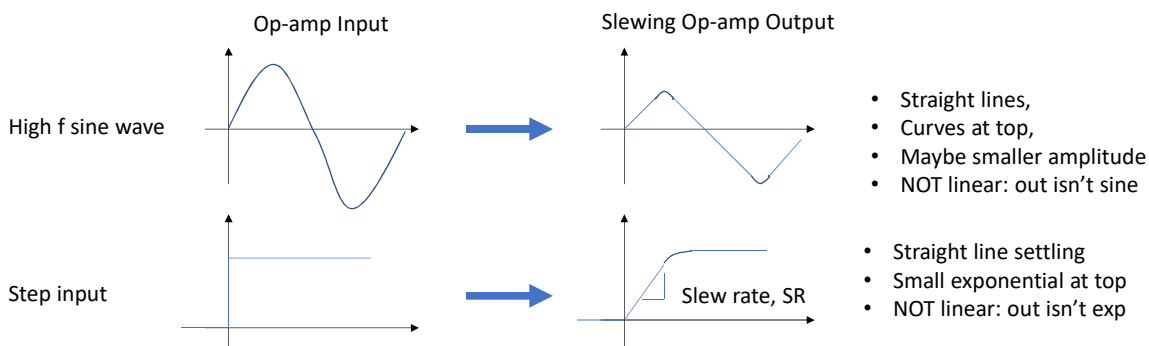
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In this video we're going to talk about a non-linear behavior in op-amps called slewing, which creates an important op-amp specification called slew rate. This is a deviation from our usual practice of confining our discussion strictly to linear approximations.

## Slewing is Non-Linear Behavior → $V_{out}(t)$ Line



- $dvO/dt$  has a “speed limit” in V/s, called slew rate
- $[V/s] = [A/F]$  because  $[A]=[C/s]$  and  $[F]=[C/V]$

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We’re going to start describing this slewing behavior by imagining that we’ve configured an op-amp for unity gain, and we’re putting a high frequency sine wave into our unity gain buffer input.

CLICK If we do that, our output won’t look like a sine wave, which is a non-linear behavior. A linear system always has a sinusoid out when you put a sinusoid in. Instead, we’ll see a triangle wave that has small curves at the top, and this triangle wave is probably going to be smaller amplitude than the square wave.

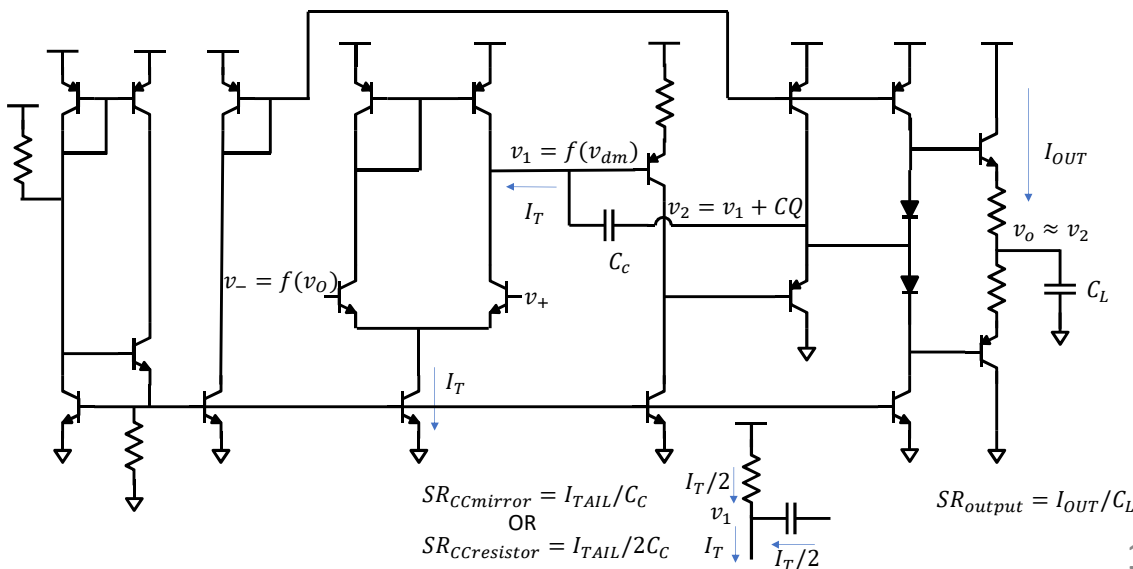
CLICK We can also see slewing if put a step input with a big amplitude into our unity gain buffer. Our response will be a straight line with a tiny exponential at the end. Again, this is not linear because a linear response to a step is a decaying exponential the whole time, a linear response doesn’t have this straight-line at the start. However, the response appears to enter a linear settling regime at the end of this straight line because there is a short exponential at the top of this response.

CLICK Looking at these two responses, you might notice that they both have straight lines in them. The slope of these straight lines is called the slew rate, and it represents the op-amp output changing as fast as it possibly can.

CLICK So, saying that another way, the slew rate is a “speed limit”  $dv/dt$ , and consequently it has units of Volts per second

CLICK It’s worth noting here that Volts per second is the same unit as Amps per Farad, which you can see because Amps are Coulombs per second and Farads are Coulombs per Volt.

## Slew if Saturating Current from a Stage



OK, so how do we get this Volts per second speed limit? The answer has to do with the fact that some op-amp stages can only provide limited current.

CLICK For example, the output stage might have some maximum current it can provide.

CLICK If that maximum current is being driven into a load capacitor, then the fastest the load capacitor can change is  $I_{OUT}/C_L$ . Remember that current over capacitance has the units of volts per second that we're looking for here. This output current can limit the slew rate, but it's uncommon because op-amp output stages are generally able to drive a lot of current. It's much more common for the slew rate to be limited by the differential stage and the compensation capacitor.

CLICK The differential stage has a tail current, and one of the defining features of emitter coupled pairs is that they steer the tail current one way or the other. However, once a tail current is fully steered, there's no way to drive the differential stage harder. At best, it can provide its tail current to a cap.

CLICK And the compensation capacitor is a big cap that needs to be charged up to move the differential stage output node. I've shown  $I_T$  being drawn out of this node, which indicates that the differential stage is fully steered to the right.



CLICK There are some subtleties in how this current results in a change in the output voltage. Let's call the differential stage output  $v_1$  and the level shift output  $v_2$ . Because there are no dynamics in the output stage,  $v_O$  will exactly track  $v_2$ , so if  $v_2$  is slew limited, then so is  $v_O$ .  $v_1$  is entirely set by the difference between the inputs, which in turn is set by how quickly  $v_O$  can move. That means for a big input change,  $v_1$  is pinned until  $v_O$  can catch up to  $v_+$  and reduce  $v_{dm}$ . So after an input that fully steers the differential stage,  $v_1$  stays the same, all of  $I_T$  passes through  $CC$ , and  $v_2$  changes linearly with time because that current charges  $CC$  and  $v_2 = v_1 + CCQ$ . That means our slew rate is set by  $I_{TAIL}/CC$  when we have a mirror loaded differential stage.

CLICK Final subtlety: this slew rate changes when the differential amplifier is resistor loaded instead of mirror loaded. If a stage is resistor loaded, then some current has to flow through the resistor to set the value of  $v_1$ . Before a big slewing step, the current in the load resistor is  $I_T/2$  because our differential mode input is zero. After a big slew-causing step,  $v_1$  can't change right away because  $v_O$  needs to catch up the change it, which means  $I_T/2$  is still forced through the load resistor, and as a result the compensation cap is only discharged by  $I_T/2$ . Summarizing: only half the tail current can get into the compensation capacitor because the other half has to pass through the load resistor to maintain  $v_1$ . This sets a third possible slew rate condition.

## Summary

- Op-amps can enter into a non-linear regime, called slewing, if the output voltage changes too fast. i.e:  $dV_{out}/dt$  has “speed limit”.
- Max change in output voltage is called the slew rate,  $SR$ . Units: [V/s]
- $SR$  can be set by output current or by compensation cap charging.

$$SR_{output} = I_{OUT}/C_L$$

OR

$$SR_{CCmirror} = I_{TAIL}/C_C$$

OR

$$SR_{CCresistor} = I_{TAIL}/2C_C$$