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Differential Circuits and Half-Circuit Analysis

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In this video series we're going to take a crucial step towards building an op-amp by analyzing differential circuits. One of the defining features of an op-amp is that it is sensitive to differences between its two inputs, regardless whether those signals are high, like 7.1V vs. 7V, or low, lik 1.1V vs 1V. Differential circuits are the key to building that functionality. We'll figure out how to analyze differential circuits in this series and get into some details in the next video series.

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Differential Representations and Differential Signals

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In this video we're going to talk about differential representations of signals, which is a way to break signals up so that we can think about their difference separately from their average value.

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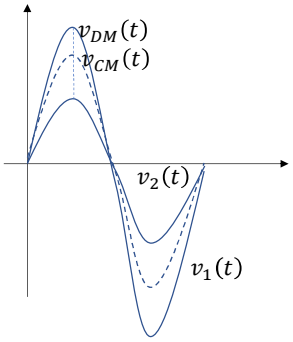
Any Two Signals have a Differential Form



Single-Ended Representation

$$v_1(t) = v_{CM}(t) + \frac{v_{DM}(t)}{2}$$

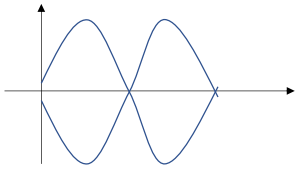
$$v_2(t) = v_{CM}(t) - \frac{v_{DM}(t)}{2}$$

Differential Representation

$$v_{CM}(t) = \frac{v_1(t) + v_2(t)}{2}$$

$$v_{DM}(t) = v_1(t) - v_2(t)$$

Purely Differential



$$v_{CM} = V_{DC}$$

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I've put a pair of signals on this slide and labeled them v1(t) and v2(t).

CLICK This drawing is called the single ended representation of signals. There are two signals, and we have a function representing each of them. I've just picked these two because they make a good picture. Any arbitrary pair of signals would work fine for the analysis we're going to jump into.

CLICK We can also make a differential representation of these signals. The differential representation is made up of two signals. A common mode, which is the average of the two single ended signals, and a differential mode, which is the difference of the two single ended signals. Again, this works for any pair of signals, we can always find an average and a difference between signals. For instance, you might notice I've used total signal notation for vCM and vDM, and that's because they don't need to be small signals. They also don't need to be in the mid-band. This math works for any two signals.

CLICK This is how the common mode and differential signals would look on the graph. The common mode is the average of v1 and v2, and the differential mode is the difference between them at every point. That would also be a sine wave, but I only highlighted it at this one point.

CLICK it's possible to invert the differential representation equations so that you can express the single ended values in terms of differential terms. V1 is the common mode plus half the differential mode, and v2 is the common mode minus the differential mode.

CLICK There's one special class of signals that I want to call out. Purely differential signals, which I'll sometimes just shorten to differential signals, have a DC value for their common mode. I've indicated that with large signal notation here. That means differential signals always have one signal moving up as the other moves down so that the average stays constant.

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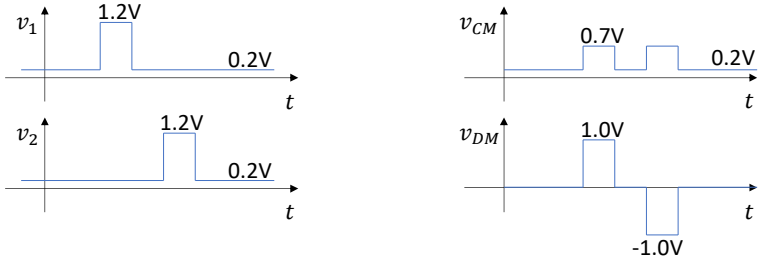
Example of Differential Representation

- Draw v_{CM} and v_{DM} for the signals below. Are they differential signals?



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Here's some practice with differential representation. I've drawn a pair of signals on the left graphs. Pause the videos and try to draw their differential and common mode representation.

CLICK The common mode is at 0.2V for most of the time, but it jumps up to 0.7V when either single-ended signal increases to 1.2V. It jumps up by 0.5V because one signal changed while the other didn't, so the average is between the two.

The differential mode signal is +1V when v1 jumps up and -1V when v2 jumps up. That's because vDM is given by v1-v2, so the increase in v1 is reflected in vDM and the increase in v2 is reflected in a decrease in vDM.

This signal is not purely differential because the common mode is changing.

… sometimes called pseudo-differential signaling

Summary

- Any two signals have a differential representation

$$v_1(t) = v_{CM}(t) + \frac{v_{DM}(t)}{2} \qquad v_{CM}(t) = \frac{v_1(t) + v_2(t)}{2}$$

$$v_2(t) = v_{CM}(t) + \frac{v_{DM}(t)}{2} \qquad v_{DM}(t) = v_1(t) - v_2(t)$$

- Differential signals have $v_{CM} = V_{DC}$.

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The Emitter Coupled Pair

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In this video we're going to start the large signal analysis of a circuit called an emitter coupled pair. This circuit is super interesting because it is sensitive to the differential mode of purely differential signals, and it doesn't care about DC shifts in the common mode.

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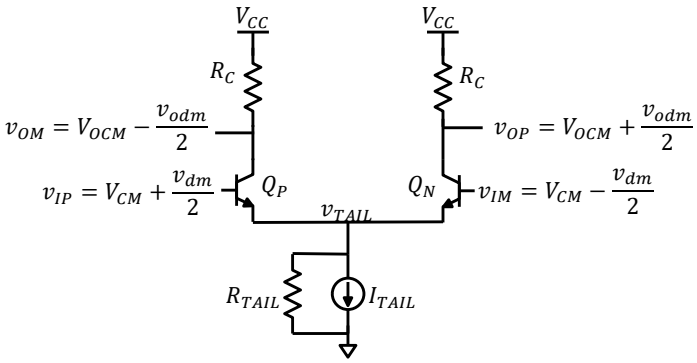
Large Signal Analysis of Emitter Coupled Pair



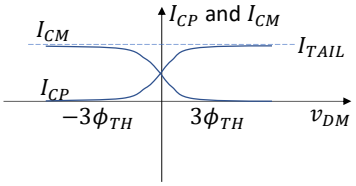
$$v_{IP} - v_{BEP} + v_{BEM} - v_{IM} = 0$$

$$v_{IP} - v_{IM} + \phi_{TH}\left(\ln\frac{I_{CP}}{I_{SP}} - \ln\frac{I_{CM}}{I_{SM}}\right) = 0$$

$$\frac{v_{DM}}{\phi_{TH}} = \ln\frac{I_{CP}}{I_{CM}}$$

$$\frac{I_{CP}}{I_{CM}} = \exp\frac{v_{DM}}{\phi_{TH}}$$

Can use $I_{CP} + I_{CM} = I_{TAIL}$ to find I_P and I_M are tanh



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I've put a picture of the emitter coupled pair on the left here. It consists of two transistors that have their emitters stuck together on a current source, so the name is pretty descriptive. I've put a resistor in parallel with the current source because no current source is perfect, that just represent the current sources output resistance. The current source is called the tail current, and the node between the emitters is called the tail node. This particular emitter coupled pair is loaded by a pair of resistors RC, though you can attach other things on top of QP and QN. We'll see some other examples next lecture.

CLICK The inputs and outputs of the emitter coupled pair are a bit complicated. It is almost always driven by a purely differential signal, which is why I'm using large signal notation for the VCM values. The two single ended inputs are referred to as the positive and negative inputs or the plus and minus inputs. I've gone with plus and minus here, which I've indicated with the subscripts P and M. The single ended outputs are called the plus and minus output, and I've indicated that the plus output is on the same branch of the emitter coupled pair as the minus input. That's an engineering choice, and we'll see soon that swapping which output you call plus vs. minus just changes the sign of your differential gain. So I could swap which of the outputs I called plus and minus without significantly changing the function of the amplifier.

CLICK We start the large signal analysis of this thing by writing a KVL look from one input,

across the tail node, and back to the other input. That gives us that vIP minus vBEP plus vBEM is equal to the other input, vIM.

CLICK Rearranging a bit, we get vIP minus vIM plus the difference between the vBE values. But we know from our work on references that we can represent vBE as phi_th time the natural log of IC/IS.

CLICK Combining the logs, assuming the IS values of the transistors match, and merging vIP-vIM into the symbol vDM, we find the differential mode voltage is proportional to the log of the collector current on the P branch divided by the collector current in the M branch.

CLICK Exponentiating that expression gets us to a relationship that I find evocative. The ratio of current in the P branch to the M branch is an exponential function of vDM over phi_TH. That means increasing the differential mode rapidly causes ICP to get bigger than ICM, and decreasing it does the opposite.

CLICK However, IP and IM have to add up to ITAIL, there's only a finite amount of current in the structure. If you combine this constraint with the relation between ICP and ICM we just derived, you can find that ICP and ICM are each hyperbolic tangent fundtions of vdm/phi_TH.

CLICK That looks like this. When vDM is very positive or very negative, then ITAIL is steered fully to QP or to QM. However, when vDM is close to zero then we see this exponential shift of current from one branch to the other. When vDM is zero, then ITAIL splits evenly between the branches. Hyberpolic tangent is a slow function, but the argument is vDM/phi_TH, and phi_TH is quite small. That means emitter coupled pairs have very small differential input ranges. If the differential mode reaches 3*phi_TH, so if there are 75mV of difference between the single-ended signals, then 96% of the signal is steered to one branch.

… usually used with a small, purely differential signal. I've indicated that w/ notation. Sometimes called v+/-.
… technically the RC aren't part of the emitter coupled pair
… current steering
… narrow input range b/c exponential

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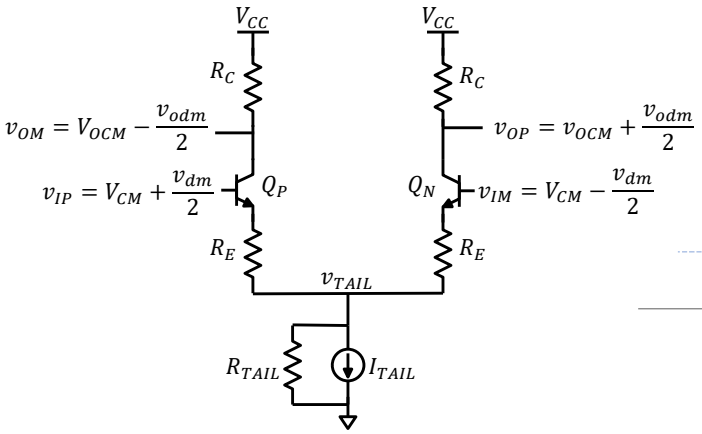
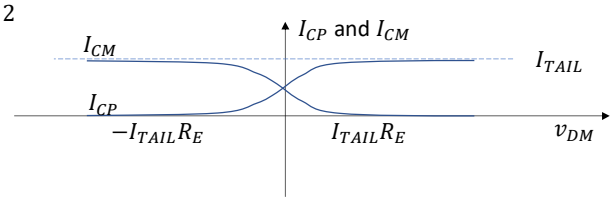
Degeneration Expands the Input Range



$$v_{IP} - v_{BEP} - v_{REP} + v_{BEM} + v_{REM} - v_{IM} = 0$$

$$(v_{IP} - v_{IM}) + R_E(I_{CM} - I_{CP}) + \phi_{TH}\left(\ln\frac{I_{CP}}{I_{CM}}\right) = 0$$

$$\frac{v_{DM}}{\phi_{TH}} = \frac{R_E(I_{CP} - I_{CM})}{\phi_{TH}} + \ln\frac{I_{CP}}{I_{CM}}$$



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The narrow input range of emitter coupled pairs is annoying, but degeneration can increase it. I've drawn an emitter coupled pair with emitter degeneration here.

CLICK We analyze the circuit in the same way, by making a KVL loop from one input to the other.

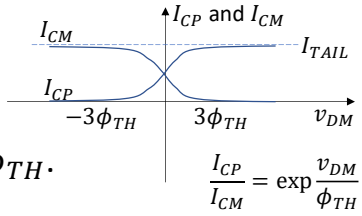
CLICK and we rearrange it the same way to find a dependence on vDM and the natural log of ICP over ICM. However, we have this third term corresponding to the voltage across the resistors too.

CLICK Rearranging a little further, we come to a transcendental equation.

CLICK However, if we graph this equation we find that it's indicates a wide, pseudo-linear steering region where ITAIL is steered between ICP and ICM. The input range is increased to ITAIL*RE in this amplifier.

Summary

- Emitter coupled pairs are only sensitive to differential signals.
- Differential voltages steer the tail current.
- The input range of an emitter coupled pair is $\pm 3\phi_{TH}$.
- The input range of a degenerated emitter coupled pair is $\pm I_{TAIL} R_E$



$$\frac{I_{CP}}{I_{CM}} = \exp\frac{v_{DM}}{\phi_{TH}}$$

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Half Circuit Analysis

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In this video we're going to perform a small signal analysis of an emitter coupled pair. We're also going to use a few neat circuit tricks to greatly simplify that analysis. Those tricks are called half-circuit analysis because they let us cut our small signal models in half.

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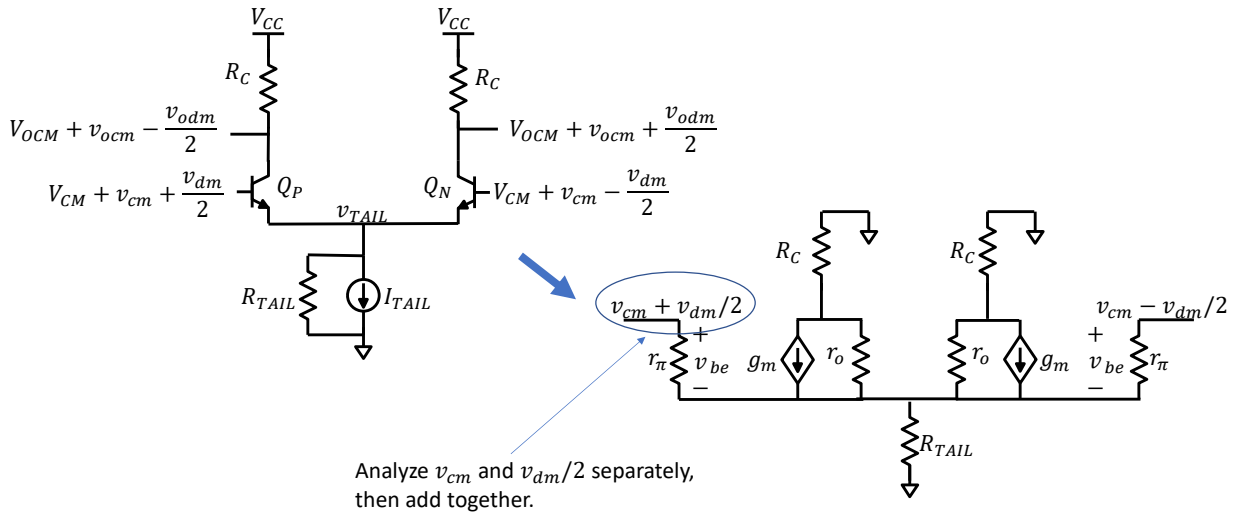
Linearity Lets Us Split CM and DM Signals



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I've drawn an emitter coupled pair on this slide and the associated small signal model. I've relaxed the input constraints we were using in the last video to allow both small signal vcm and vdm variations on top of the DC common mode. That means we'll be able to analyze any arbitrary pair of small signals on top of a DC common mode. Note that we're now relaying on two assumptions about our signals: we assume that we have small signal deviations from a DC common mode, so we're combining small signal analysis and differential analysis.

We could solve this small signal model, it's not much more complicated than a cascode, but this model has some oddities. If we think of the circuit in terms of single-ended signals, then it has two inputs, and we don't have any analysis tools that deal with multiple input systems. Even if we use a differential representation, there are two different signals that can change the circuit's behavior: the common mode signal and the differential mode signal.

CLICK Fortunately, our small signal model is linear. That means we can break the input signal into vcm and vdm, analyze those two signals separately, then add the results together to find the output. The common mode analysis and the differential analysis will each have one input and one output. Breaking up the differential and common mode signals like this is called half-circuit analysis. We'll see why in a minute.

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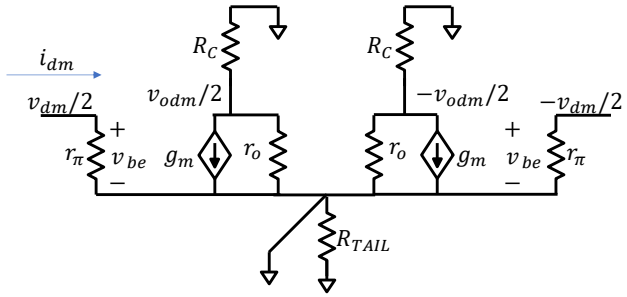
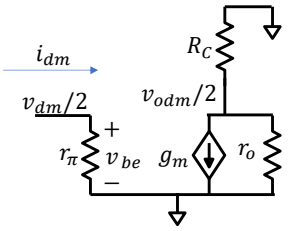
Differential Half Circuits





Net current into R_{TAIL} must be zero!

If tail node doesn't change, it's virtually grounded.

$$a_{vdm} = \frac{v_{odm}}{v_{dm}} = \frac{v_{odm}/2}{v_{dm}/2} = -g_m(R_C||r_o)$$

$$r_{indm} = \frac{v_{dm}}{i_{dm}} = \frac{v_{dm}}{(\frac{v_{dm}}{2})/r_\pi} = 2r_\pi$$

$$r_{outdm} = \frac{v_{odm}}{i_{odm}} = \frac{v_{odm}}{(\frac{v_{odm}}{2})/(R_C||r_o)} \approx 2R_C$$

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We're going to look at purely differential small signal inputs first, and that's going to result in us drawing something called the differential half-circuit.

CLICK The big thing to notice when we draw diferential half-circuits is that no current will ever flow into RTAIL. Because our input signal is purely differential and every element is perfectly linear, any increase in current on the left side of the circuit will be absorbed by an equal decrease on the right side of the circuit. That means differential current flows into one base or collector of an emitter coupled transistor, then out of the other base or collector. So differential currents flow across the small signal model, but never down the tail.

CLICK If there's no small signal currents flowing in RTAIL, then the tail node never changes voltage. And if a node doesn't change in a small signal model, that's the same thing as it being grounded. Said another way, small signal models represent deviations from a large signal bias point, so nodes that don't deviate are small signal grounds.

CLICK That means we can virtually ground this tail node. If we do that, then the analysis of this circuit becomes much easier because the left side and the right side don't interact anymore. So we can just analyze the left side of this structure, which is called a differential half-circuit.

CLICK Our half circuit looks like this. We've copied over all the elements and node voltages from the left side of the circuit. We know that the right side of the circuit will do exactly the same thing as this model because it's identical. The only difference is that the input is negative instead of positive. This half circuit is obviously a common emitter, and we know how to analyze those.

CLICK The voltage gain for this half-circuit is given by the differential output voltage divided by the differential input voltage. Out half circuit doesn't tell us vodm or vdm, instead it has vodm/2 and vdm/2, but the ratio of those two values is the same thing. Because the circuit is a common emitter, we know that vodm/2 over vdm/2 is going to be –gm*(RC||ro).

CLICK The input impedance of the differential half circuit is a bit weirder. It's given by the differential input voltage over the differential input current. However, the input voltage is split between the left and right half-circuits, while the differential current is shared since flows from left to right. We know the current that flows in our half-circuit is given by vdm/2 divided by rpi, and comparing that current to vdm tells us that rindm is 2rpi. That's twice as big as we'd expect, but that result comes from how we define differential voltages and currents, not from any change in the transistor behavior.

CLICK rout has similar behavior, which means we see an output resistance of about 2RC, instead of just RC for a normal common emitter.

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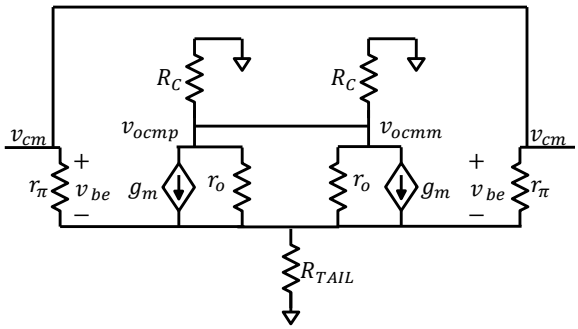
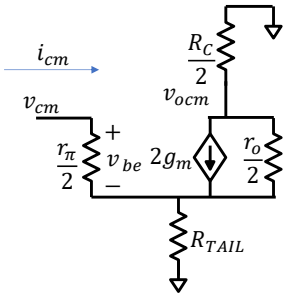
Common Mode Half Circuits



Voltage $v_{ocmp} = v_{ocmm} = v_{ocm}$

If voltages are the same, can virtually short nodes.



$$a_{vcm} = \frac{v_{ocm}}{v_{cm}} \approx -\frac{R_C/2}{R_{TAIL}} = -\frac{R_C}{2R_{TAIL}}$$

$$r_{incm} = \frac{v_{cm}}{i_{cm}} = \frac{r_\pi}{2} + (\beta + 1)R_{TAIL}$$

$$r_{outcm} = \frac{v_{ocm}}{i_{ocm}} \approx \frac{R_C}{2}$$

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The common mode half circuit has to be analyzed a bit differently from the differential half circuit.

CLICK I made some deliberately obtuse notation on this slide by calling the two output nodes by different names. However, we know the input to either side is going to be identical and that our differential structure is perfectly symmetrical. That means the output nodes are always going to be at the same voltage.

CLICK If those votlages are the same, then we can short the left and right output nodes together without changing anything about our analysis. The same is true for the two inputs, which also have the same voltage. If we had other nodes that had the same voltage on the left and the right, then we could short those too.

CLICK This is what the circuit looks like with the nodes shorted. And we can observe that with these nodes shorted, lots of elements are in parallel. For instance, both the left and right rpi resistors have vcm on the top and the tail node on the bottom. This lets us combine them in parallel.

CLICK Doing so lets us simplify our circuit quite a bit to find the common mode half-circuit. Note that common mode current does flow into RTAIL, unlike differential mode current.

Common mode current flows into the bases and collectors of both transistors and down into RTAIL. This circuit is obviously a common emitter with degeneration, which means we can analyze the common mode amplifier parameters pretty easily.

CLICK First, the common mode gain is given by vocm over vcm. In a common emitter with degeneration that's about the emitter resistance over the collector resistance. So we get RC over 2RTAIL. Because RTAIL is a big current source output impedance, the common mode gain is usually quite small. Note that factor of two comes from shorting the two output nodes together to reduce RC, which is different than how the differential mode gain worked; we don't have to worry about the same factors of two that we saw in the differential half circuit because we see the full vocm and vcm in this half circuit.

CLICK The common mode input resistance is given by the common mode input votlage over the common mode input current. For a degenerated common emitter, that's given by the resistor in the rpi position, rpi/2 for us, plus beta+1 times the resistor in the emitter position, RTAIL in our case. Note that the beta in this case is made up of 2*gm multipled by rpi/2, but the factors of two cancel out to give us the same beta.

CLICK Finally, the common mode output resistance is given by RC/2 in parallel with the big impedance seen looking down into a degenerated common emitter.

It's worth noting that the amplifier parameters of this resistively loaded emitter coupled pair are different for common mode and differential signals. This is true in general for any amplifier parameters. For instance, there are separate sets of differential and common mode open circuit time constants. I find it kind of magical that this structure has a different bandwidth for differential signals and common mode signals, but it's true.

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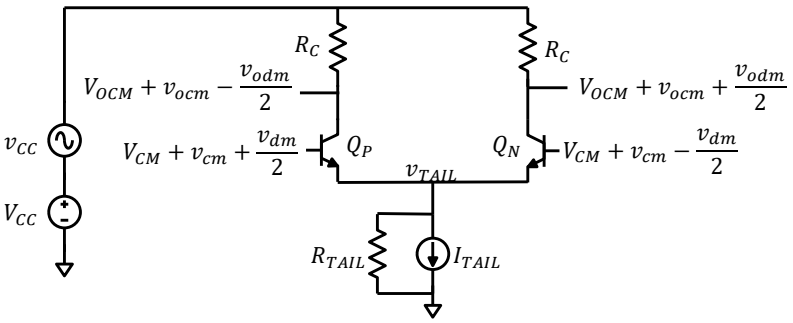
Rejection Ratios Measure Differential-ness



Common Mode Rejection Ratio

$$CMRR = \frac{a_{vdm}}{a_{vcm}}$$

Power Supply Rejection Ratio

$$PSRR = \frac{a_{vdm}}{a_{vcc}} \quad \text{where} \quad a_{vcc} = \frac{v_{ocm}}{v_{cc}}$$

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When we build differential amplifiers we usually want them to be sensitive to differential signals and insensitive to common mode signals. Amplifiers have a few figures of merit that help us measure how well we've done in that goal.

The first of these is the common mode rejection ratio, which is the ratio of the differential voltage gain to the common mode voltage gain. It tells us how much the amplifier will reject common mode changes at its inputs. We want it to have a high value so that differential signals get lots of gain and common mode signals get very little.

The second of these is the power supply rejection ratio, which measures how much the power supply can affect our output. When the power supply changes, it results in common mode changes in the output because the power supply is common to both branches of the amplifier. We can define a gain from the power supply to the output, which we'll call avcc, by imagining that we have a small signal input test source on the power rail. I've drawn that situation the right. We define the power supply rejection ratio as the differential mode gain divided by avcc. You'll also see the power supply rejection ratio defined relative to a single-ended output sometimes.

Summary

- Generate differential half-circuits by virtually grounding the symmetrical center node of a circuit.
- Generate common-mode half-circuits by shorting non-tail nodes and combining elements in parallel.
- Common mode and differential mode amplifier parameters differ.
- Common mode rejection ratio is a_{vdm}/a_{vcm}.

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Half Circuit Analysis Examples

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E151 – Analog Circuit Design

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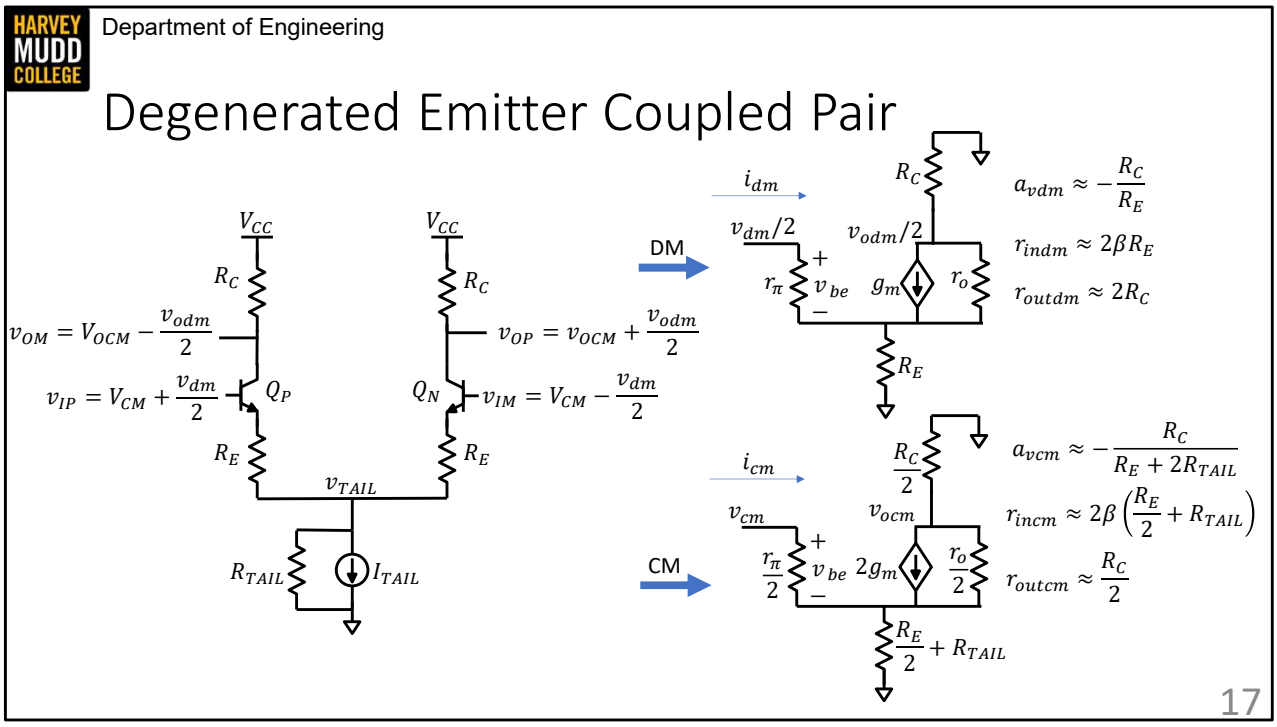
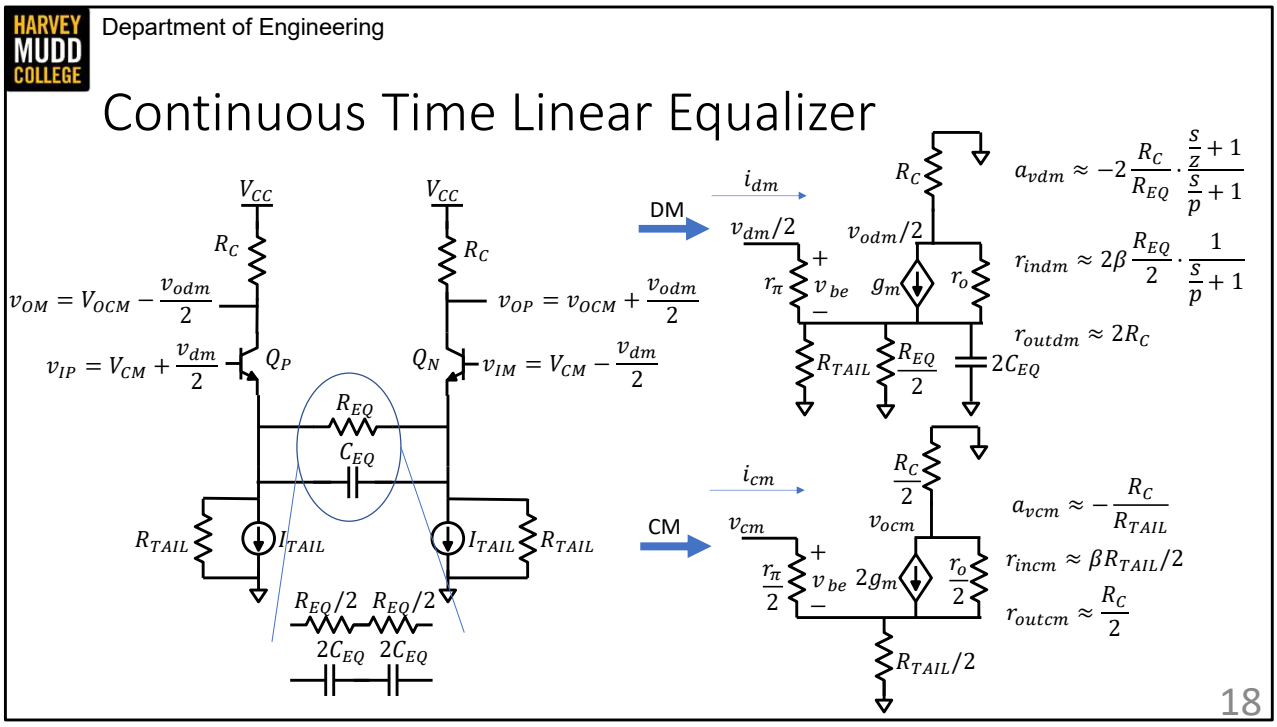
In this video we're going to get some practice with half-circuit analysis.



I've drawn an emitter coupled pair with degeneration on the left. Pause the video and find the common mode and differential mode half circuits, then calculate gain, input impedance and output impedance for both the common mode and differential circuits.

CLICK The tail node here is a differential ground, so we can analyze the left side of the structure, which includes RE as a degeneration resistor. That means the differential half-circuit is a common emitter with degeneration. So avdm is –RC/RE, rindm is 2*beta*RE where the factor of two is coming from the fact we apply vdm/2 at the half-circuit input, and routdm is 2RC.

CLICK The common mode half circuit looks pretty similar, but most components are halved or doubled by the common mode behavior of the circuits, and the degeneration resistor is RE/2+RTAIL. This is also a common emitter with degeneration, so avcm is –RC/(RE+2RTAIL), which is quite small, rincm is 2*beta*(RE/2+RTAIL), and routcm=RC/2 in parallel with the big CE with degeneration resistance.



This circuit, called a continuous time linear equalizer, is somewhat trickier than the last one.

Pause the video and try to draw the common mode and differential half-circuits. Feel free to analyze the DC gain, input impedance and output impedance too. The dynamic response is a bit complicated, and I'm not going to go fully into it on this slide, but I don't want to stop you from deriving it if you feel like it. One important hint is to consider carefully where the differential virtual ground is in the circuit, and to note that some parallel or series equivalent circuits might help you find it.

CLICK OK to solve this circuit we need to find the differntial virtual ground, and if we meditate for a bit we can see that it is in the middle of the equalization resistor and capacitor. The easiest way to see that is is the replace the equalization R and C with two series elements that have the same total value. The node in the middle of them has to be a differential virtual ground because any current that flows into it on the left has to flow out on the right.

CLICK Knowing that, we can make a differential half-circuit that looks like a common emitter with complex degeneration. The gain is given by RC/ZE, which can be broken into a DC RC/2REQ multiplied by a pole-zero pair. The zero is at a lower frequency than the pole,

so this structure has an increase in its differential gain at high frequency. That's because the equalization capacitor shorts out REQ, which removes the resistive degeneration from the amplifier. The input impedance is beta*ZE, which looks like beta*REQ/2 at DC, and rolls off as the capacitor shots out REQ. Finally, the output impedance just looks like 2*RC.

CLICK The common mode is much tamer because the equalization resistor and cap are shorted out. The emitter voltages of QP and QN are the same in a common mode circuit, and no current flows in the equalization network. That means our common mode circuit is a normal CE with degeneration. The gain is –RC/RTAIL, the input impedance is about beta time RTAIL/2 and the output impedance is RC/2.

Summary

- Analyze differential circuits by cutting circuits into common mode and differential half-circuits.
- You can virtually cut elements in half to make symmetry points for differential half-circuit analysis.
- Continuous time linear equalizers give you a gain bump at high frequencies. (Though their input impedance drops at high f too.)