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Current Mirrors

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In this video series we're going to study a transistor structure that is used for biasing amplifiers and active loads. The structure makes copies of current, so it's called a current mirror. Current mirrors are crucial amplifier building blocks, and being able to recognize them will let you pick apart tricky schematics. We can also cover them in one lecture, which is important as we lead up to the midterm: we don't want to be introducing big long analyses right now.

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The Simple Current Mirror

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In this video we're going to get started with current mirrors by analyzing the simplest one, which is conveniently called the simple current mirror. By the way, that name is a warning: there might be a few complicated current mirrors out there, so let's enjoy our time with this one.

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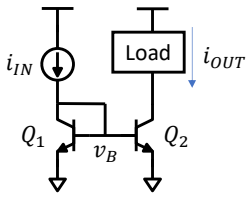
Current Mirrors Set $i_{OUT} \approx i_{IN}$



$$i_{C1} = I_{S1}\left(\exp\left(\frac{v_B}{\phi_t}\right) - 1\right) \leftrightarrow v_B = \phi_t \ln\left(1 + \frac{i_{C1}}{I_{S1}}\right)$$

$i_{C2} = i_{C1}$ because $v_{B2} = v_{B1} = v_B$

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The simple current mirror is pictured on the left here. The title gives away its big trick, which is that the current iOUT is forced to be the same as the iIN current source.

CLICK The heart of that trick is that vB is a one-to-one function of iC. So the iIN current source creates some amount of iC1 in the diode connected Q1, and we can invert the iC1 equation to find that vB is set to the value that produces iC1 of current.

CLICK That means the iC1 current must match the iC2 current because both transistors share the same base voltage, vB, which we already know is appropriate to create iC1. Great! Now all we need to do is find the relationship between iC1 and iIN.

Before we do that, I want to take a tiny aside to mention that current mirrors are an interesting structure because you could argue that they use a technique called predistortion. Q1 converts iIN to vB through a non-linear function, and Q2 uses the inverse of that non-linear function to create iOUT. So we're using Q1 to pre-distort the iIN signal. That means we're deliberately leveraging non-linear operation of these devices, and we don't rely on a small signal model here. That's cool! It's also why I've been using total signal notation throughout.

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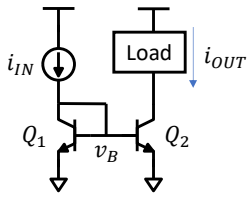
BJT Current Mirrors Have Small Errors



$i_{C1} = \beta i_{B1}$ b/c Q_1 guaranteed in FAR by diode connection

$i_{B1} = i_{B2}$ b/c Q_1 and Q_2 have the same v_B

$i_{IN} = i_{C1} + i_{B1} + i_{B2}$

$i_{IN} = i_{B2}(1 + 1 + \beta)$

$i_{OUT} = \beta i_{B2} = i_{IN} \frac{\beta}{\beta + 2}$

$\epsilon = \frac{\beta}{\beta + 2} \approx 98\%$ for simple current mirrors

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Alright, back to relating iC1, which is equal to iC2, to i_IN.

CLICK First, we observe that iC1 has to be beta time iB1 because Q1 is in forward active. We know it's in forward active because it's diode connected, and diode connected devices are either in forward active or cutoff.

CLICK Second, we recall from the previous slide that iB1 has to be the same as iB2 because vB is the same on both devices. Note that this equation is assuming Q1 is identical to Q2, which isn't all that safe of an assumption in normal transistor manufacturing processes. Mismatch in Q1 and Q2 results in current mismatch, and we'll look at that in more detail later.

CLICK Then we write KCL at the vB node, noting that two base currents and one collector current flow out of it, while iIN flows in.

CLICK We can substitute values in for iC1 and iB1

CLICK and finally note the relation between iB2 and iC2 and rearrange a bit to get this final relation between iIN and iOUT. There's a slight mismatch between iIN and iOUT that comes from the base currents stealing a bit of iIN.

CLICK We capture that in an important current mirror parameter called the error factor, or epsilon. It's the ratio of iOUT/iIN, and for simple mirrors it's about 98%. A 2% error is actually quite high, and there are lots of trickier mirrors that reduce this error. We're only going to study one of them in detail because this error is somewhat unique to BJTs: other transistors, like MOSFETS, mostly don't have base current. As a result, this type of analysis -- which I call and error problem, by the way – is almost never done in the real world. That means I'm not going to hold you responsible for doing any, which is kind of a shame because it's sort of satisfying analysis to chase KCL around a circuit.

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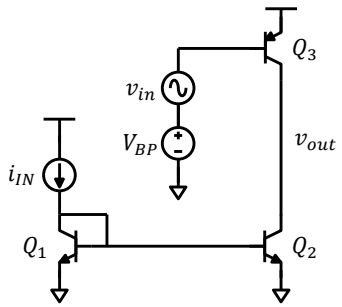
Current Mirrors Let Us Bias Active Loads



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Great, so now we know how a current mirror works and that it basically makes iOUT=iIN, within a small margin of error. Why do we care?

The answer is that current mirrors are very handy for biasing circuits, especially circuits with active loads. Here we've used the Q1/Q2 current mirror to set the collector current of Q3, which we could only do with tricky graphical analysis before. We still need to get VBP right for this circuit to work, but we don't also have a sensitive bias voltage on the base of Q2. It turns out that current mirrors can help bias Q3 as well, we'll see more on that later. We've also introduced a new problem, which is making the iIN current source. Though we generally only control voltages in lab, making a current source that only produces one current using transistors is reasonably straightforward. More on that later too.

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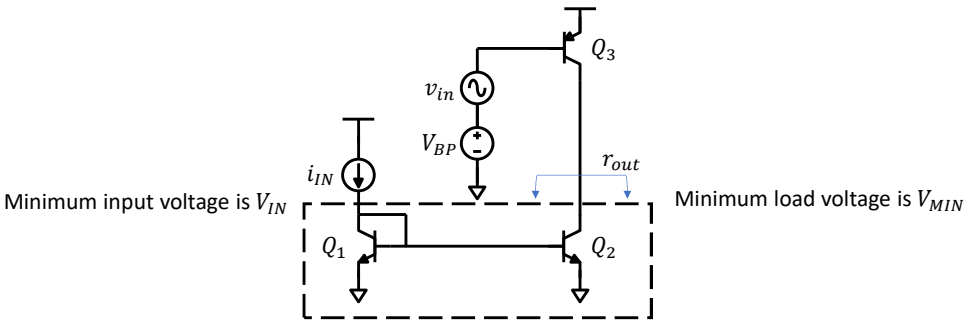
Current Mirrors Described By Parameters



For this mirror: $V_{IN} = V_{BEON1}$ $r_{out} = r_{o2}$

$V_{MIN} = V_{CESAT2}$ $\epsilon = \frac{\beta}{\beta + 2}$

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We've already talked about error as a parameter of current mirrors, but seeing them in this application as active loads is a hint at a few other important current mirror parameters. It's helpful to define the boundaries of our current mirror when we talk about these parameters, so I've included a dotted line that surrounds our current mirror in the schematic above. The box has an input wire on the left, where iIN enters the mirror, and we expect that current to be copied to the output wire on the right.

CLICK In order for that to happen, we need to make sure to maintain some minimum voltage on the input wire to keep the mirror devices in forward active. That voltage is called VIN, and it's a current mirror parameter.

CLICK Similarly, we need to keep all the devices in the mirror in forward active, which means there will be some minimum voltage on the output wire too. That voltage is called VMIN.

CLICK Finally, because mirrors are used as active loads so often, it's important to calculate their small signal output impedance, rout. Note that this is a small signal parameter, while VIN and VMIN are large signal parameters.

Pause the video and try to find VIN, VMIN and rout for this simple current mirror.

CLICK VIN is VBEON1 because the diode connected device needs to stay in forward active, which requires vB be high enough to turn on the Q1 base-emitter diode. VMIN is VCESAT2 because we need to keep Q2 from saturating. It's guaranteed to be in forward active by vB unless its collector voltage dips too low. An output source connected to the output of the mirror would just see ro2 to ground because the Q2 gm generator is shut off by the diode connected transistor connecting the base to ground. That means rout is just ro2.

… this sets iC in Q3 to be the same as Q2, which biases the whole circuit.
… We still need to get VBP just right so that it is tell Q3 to have the same current as Q2, and we still need to figure out how to make i_IN

Summary

- Current mirrors set $i_{OUT} \approx i_{IN}$.
- BJT current mirrors have small error factors, which we label ϵ
- Current mirrors can help us bias actively loaded amplifiers.
- Current mirror design parameters are V_{IN}, V_{MIN}, ϵ and r_{out}

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Current Mirror with Beta Helper

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In this video we're going to analyze another current mirror, which is called a current mirror with a beta helper. We're doing this mostly to introduce the idea of a beta helper, which is a trick that shows up all over BJT designs. We're going to do one more error analysis in this video because it helps explain what the beta helper is doing, but remember that I don't think being able to do error analysis is super important to the engineers of today.

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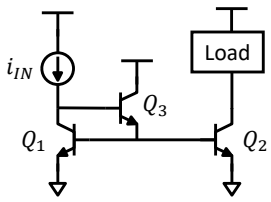
Beta Helpers Help Source Base Current



$$i_{OUT} = i_{C2} = \beta i_{B2}$$

$$i_{E3} = i_{B1} + i_{B2} = 2i_{B2} = (\beta + 1)i_{B3}$$

$$i_{IN} = i_{C1} + i_{B3}$$

$$= \beta i_{B2} + \frac{2}{\beta + 1} i_{B2}$$

$$= i_{OUT}\left(1 + \frac{2}{\beta^2 + \beta}\right)$$

$$\epsilon = \frac{\beta^2 + \beta}{\beta^2 + \beta + 2} \approx 99.98\%$$

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Q3 in this circuit is called a beta helper, and it helps to source the base current for Q1 and Q2 so that iIN doesn't see that base current pulled away. You might notice that Q3 looks a bit like an emitter follower, and that's a good observation. It's acting like a voltage buffer, creating a copy of its base voltage at its emitter, which makes iIN see a much bigger input impedance. That means Q1 is still kind-of diode connected like the current mirror, just in a fancy way with a voltage buffer in the middle.

If you want to try an error calculation, you can pause the video and give this one a shot. That's optional though because I'm not holding your feet to the fire for error calculations, but this one is a reasonably satisfying and quick problem.

CLICK We start our analysis by noting that iOUT is equal to iC2, which is beta time iB2 because we usually assume everything is operating in forward active in a mirror.

CLICK The emitter of Q3 sees provides both base currents to Q1 and Q2, and those base currents are the same because the base voltage on Q1 and Q2 is the same. We can also relate those base currents to the base current of Q3, by noting that iE3 is equalt to beta+1 times iB3.

CLICK KCL at the collector of Q1 lets us see that iIN is equal to iC1+iB3.

CLICK and we can use substitutions from the second line to express iC1 as beta times iB2 (because iB2 is the same as iB1) and iB3 in terms of iB2.

CLICK We can rearrange and use our relation between iC2 and iB2 to write iIN in terms of iOUT.

CLICK Finally, a little more rearranging gives us our error factor, which is about 99.98%. 0.02% is an acceptably low error, and we have our Q3 voltage buffer to thank for it.. Thanks, beta helper!

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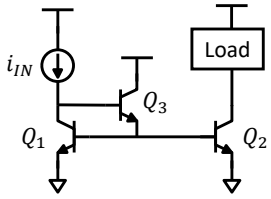
Beta Helpers Increase V_{IN}



$V_{IN} = 2V_{BEON}$
$V_{MIN} = V_{CESAT}$
$r_{out} = r_o$

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Calculating the other current mirror parameters for this current mirror is pretty straightforward. Pause the video and try to find VIN, VMIN and rout.

CLICK VIN has increased to 2VBEON because we need to keep both Q1 and Q3 in forward active. VMIN is still VCESAT because we're only worried about Q2 getting into saturation. rout is still ro because the output of the emitter follower just sees the collector of Q2 on its path to ground. We've paid a bit of VIN to have our good error performance, and many current mirror designs try to break that tradeoff.

Summary

- Beta helpers source base current.
- The beta helper in this current mirror increased V_{IN}.
- Current mirrors generally come with similar design tradeoffs.

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Cascode Current Mirror

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In this video we're going to analyze cascode current mirrors because they get used quite a bit. These are interesting because of their high rout, which will give us a chance to try small signal analysis on mirrors.

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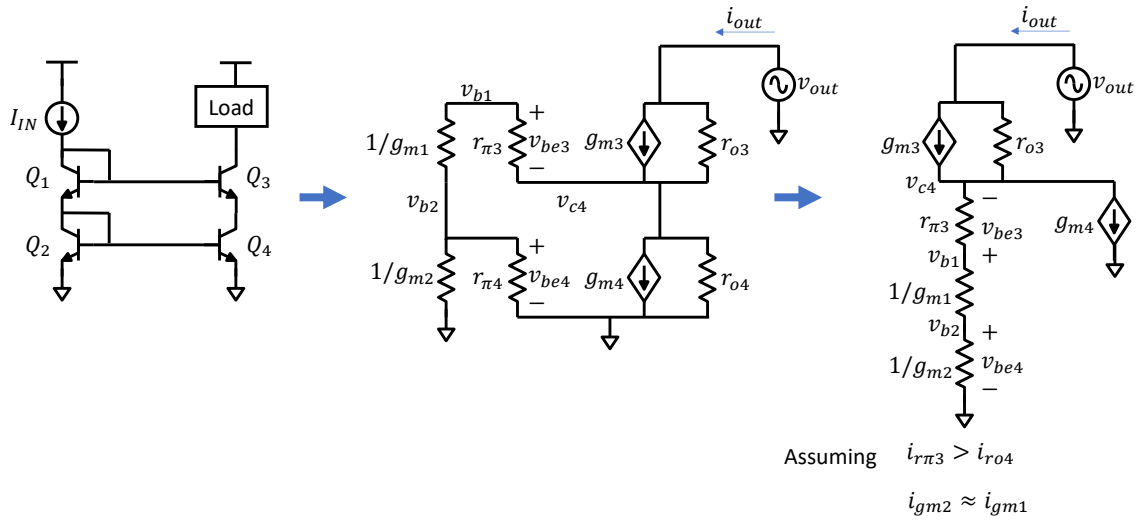
Cascode Current Mirrors Have High rout.



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A cascode mirror appears on the left of this slide. I just promised that cascode mirrors have high rout and we're going to prove it on the next two slides. Doing so will require small signal models. Pause the video and try making a small signal model for the cascode current mirror pictured here. Note that I've labeled IIN as a large signal current source, which is typical when you're trying to create stable bias currents using mirrors. Note also that the diode connected devices have turned into 1/gm resistors.

CLICK Here's a complicated looking small signal model, where I've just substituted our hybrid pi model in for the large signal circuit. Note that IIN becomes an open circuit here. Note also that this is a mess!

CLICK Here's my attempt to simplify it. I made two assumptions to do so, which is that not much current flows into ro4 instead of rpi3 – so I left ro4 as an open circuit – and that not much current flows into rpi4 instead of 1/gm2, so I left rpi4 out of the drawing. This model is troubling because it's not one of our small signal patterns, which might mean that we have to reinvent the wheel by grinding away with KVL and KCL in the circuit.

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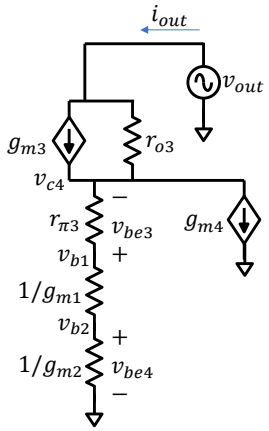
Cascode Current Mirrors Have High r_{out}



$$i_{out} = i_{r\pi 3} + i_{gm4}$$

$$i_{gm4} = g_{m4}\left(\frac{i_{r\pi 3}}{g_{m2}}\right) \approx i_{r\pi 3}$$ Makes sense b/c current mirror

$$i_{out} \approx 2i_{r\pi 3}$$

$$-v_{be3} \approx \frac{i_{out}}{2} r_{\pi 3} \approx v_{c4}$$ Redoing left-right pattern w/ $i_{out}/2$

$$i_{out} = i_{gm3} + i_{ro3}$$

$$= \frac{g_{m3} r_{\pi 3}}{2} i_{out} + \frac{v_{out} - i_{out} r_{\pi 3}/2}{r_{o3}}$$

$$r_{out} \approx \frac{\beta_3 r_{o3}}{2}$$

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I'm going to find rout on this slide, but I encourage you to pause the video and take a run at it first. This is a tricky small signal problem, and it's easier if you make a bunch of assumptions. I'm going to do that in my solution to focus in on the insights you can take away about the circuit's operation. However, if you want to solve it in all it's glory, then you will get good practice with small signal models. Pause the video now if you want to try.

CLICK Our usual left-right pattern analysis assumes all of our test current flows in the tail resistance below the current source, but that isn't true here. Instead we have this additional gm4 source dangling off the side of our analysis and eating up part of iout. Finding that igm4 and kicking it out of our analysis will make our life easier.

CLICK Fortunately, its control voltage is pretty easy to find. We know that vbe4 is going to be whatever current is flowing in the rpi3 branch times 1/gm2, and we further know that igm4 is just gm4 times that quantity. Q2 and Q4 were designed as part of a current mirror, so it's likely that gm4 is pretty close to gm2 (though relaxing that constraint lets you play some neat biasing tricks), which means that igm4 is about equal to irpi3. That means the current that enters the vc4 node just splits in half between the two branches. That seems like a suspiciously convenient result, and there's a good reason for it. Q2 and Q4 are a current mirror, and current mirrors guarantee that the total signal iIN matches the total signal iOUT, which means that they make the same guarantee for small signals that are part

of a total signal. The current is splitting in half because the Q2/Q4 current mirror is forcing current in both Q2 and Q4 collectors to be equal.

CLICK OK, so after this, we can just redo the usual left-right pattern analysis using a reduced valued of iout passing through rpi3. I've included this line to indicate a simplifying assumption I'm making for the rest of the analysis, which is that rpi3 is bigger than 1/gm1+1/gm2, so we can just ignore those resistors when we calculate vc4. That lets us say that vc4 is about the same as vbe3.

CLICK So we write KCL at the iout node on top of the structure

CLICK Then substute in the gm3 current value based on vbe3 and the ro3 current value based on the difference between vout and vc4, which is close to vbe3. At this point, the equation looks like our usual right-left patter equation with just a few funny factors. However, you can see that clearing the ro3 from the denominator of the rightmost term will give us a factor of beta3*ro3/2 times iout in the leftmost term.

CLICK And that term winds up dominating the equation, so our final expression for output resistance of a cascode mirror will be about beta3*ro3/2. That's half the resistance of a cascode amplifier, and it's cut in half by the action of the Q2/Q4 mirror.

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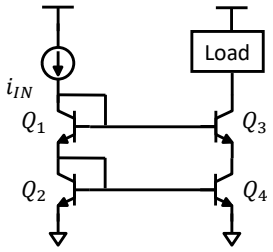
Other Cascode Mirror Parameters Middling



$$\epsilon = \frac{\beta^2}{\beta^2 + 4\beta + 2} \approx 96\%$$

$$V_{IN} = 2V_{BEON}$$

$$V_{MIN} = V_{BEON} + V_{CESAT}$$

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Epsilon is also involved for a cascode amplifier so I've just included it on this slide. It's worth noting that the error is pretty middling. The other cascode amplifier parameters are easier to find. Pause the video and find VIN and VMIN.

CLICK VIN is 2VBEON to keep Q1 and Q2 in forward active. In general, diode connected devices require a VBEON drop across them, just like a diode. VMIN is a bit tricker. It's VBEON+VCESAT because the emitter of Q3 is pinned to VBEON by Q1 and Q2. You pick up VBEON going up Q2, and then an addition VBEON going up Q1, then you drop a VBEON on the base-emitter junction of Q3. Finally, you need to keep the output at least VCESAT above the emitter to keep Q3 from saturation. This practice of navigating around a large signal circuit by climbing up and down VBEON values is really common, you should look for opportunities to do it.

Summary

- Cascode current mirrors have a high $r_{out} = \beta r_o/2$.
- Other cascode mirror parameters are only OK
  - $V_{IN} = 2V_{BEON}$
  - $V_{MIN} = V_{BEON} + V_{CESAT}$
  - Error factor ~96%
- Beware of tricky small signal models that defy our patterns.