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Introduction to Amplifiers

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E151 – Analog Circuit Design

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In this video series we're going to talk about our first amplifier and some of the design specifications that we'll use to categorize amplifiers for the rest of the class. It's a milestone, and it means that you'll be building amplifiers very soon. Today we'll be going over a crucial small signal model of amplifiers, and we'll talk about some large signal considerations that sneak into this model in the next video series.

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The Common Emitter Amplifier

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In this video we're going to talk about our first amplifier circuit, the common emitter amplifier. Unbeknownst to you, we've already look at the common emitter, so we'll be revisiting an old circuit in a new light.

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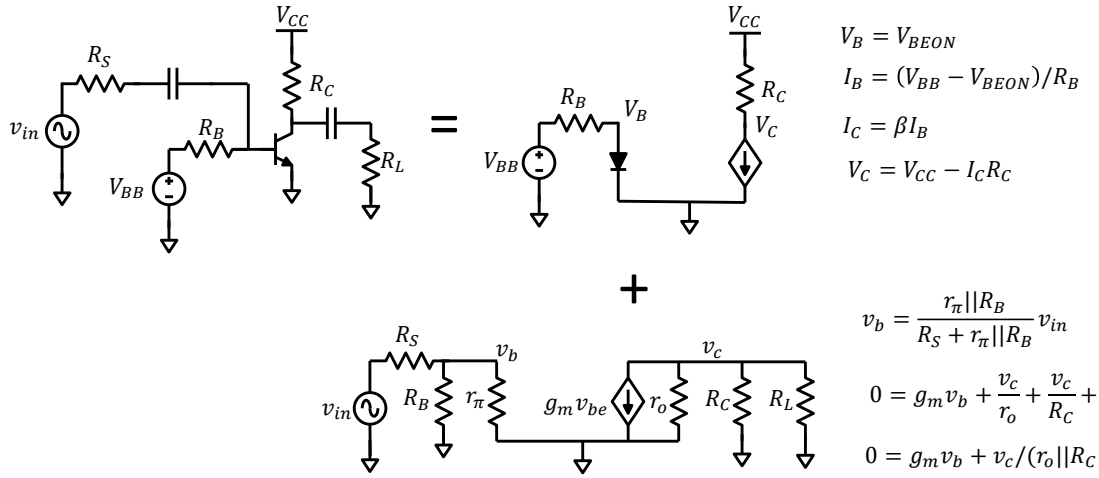
We've Already Seen Our First Amplifier



$$V_B = V_{BEON}$$
$$I_B = (V_{BB} - V_{BEON})/R_B$$
$$I_C = \beta I_B$$
$$V_C = V_{CC} - I_C R_C$$

$$v_b = \frac{r_\pi || R_B}{R_S + r_\pi || R_B} v_{in}$$
$$0 = g_m v_b + \frac{v_c}{r_o} + \frac{v_c}{R_C} + \frac{v_c}{R_L}$$
$$0 = g_m v_b + v_c/(r_o || R_C || R_L)$$
$$v_c = -g_m\,(r_o || R_C || R_L) \frac{r_\pi || R_B}{R_S + r_\pi || R_B} v_{in}$$

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This familiar circuit in the upper left is the first amplifier we are going to study, but now we're going to refer to it as a common emitter amplifier. It has that name because the emitter is grounded. It's the same circuit that we studied when we were calculating large signal bias points for BJT circuits, but I've added a small signal input with a source resistance Rs that is connected to the base through a capacitor. I've also added a load, Rl, that is connected to the collector through a capacitor. Connecting a series capacitor to a signal in this way is called AC coupling because only high frequency signals can pass through the capacitor; the capacitor will have infinite impedance for DC signals, acting like an open circuit, and low impedance for high frequency signals, acting like a short. This type of connection is called AC coupling a signal.

CLICK We can see the effect of AC coupling in our large and small signal versions of the circuit. The large signal circuit excludes the AC coupled branches because the capacitors are open circuits at DC. The small signal circuit shorts the capacitors and voltage sources, which results in RB falling in parallel with rpi and RC falls in parallel with RL. The collector resistance in parallel with the load resistance is sometimes troubling to students, but I find the circuit less strange if I remember that the small signal circuit is only representing changes from the large signal circuit.

CLICK The derivation of the large signal bias point is the same as we've seen before. The

base voltage is VBEON, the base current is set by the the voltage across RB, and the collector current is set by beta times IB.

CLICK We're going to take a more careful look at the small signal circuit, and we're going to start by finding vb, which controls the current in the dependent source because the emitter is grounded. vb is just given by a divider between rpi in parallel with RB and the source resistance.
CLICK the collector voltage is the voltage applied across the load, so it's the output of the circuit. That means our ultimate goal is to find a relationship between our input, vin and our ouptu vc. We write KCL at this node to start finding that process. Immediately, something looks a bit weird: if we follow our instincts, it looks like all the currents should be leaving the node. A positive vc will cause current to flow down ro, RC and RL, and the dependent source insists that current flows down it if vbe is positive. However, that leads to a KCL equation with a zero on one side, so either vc or vb has to be negative, and in turn that either current is flowing up the dependent source or up the resistors. That's weird.

CLICK We can see that more clearly if we gather the resistor terms into a parallel combination.

CLICK Finally, we can rearrange that expression and substitute in for vb to find that vc is equal to some coefficient times vin. We refer to that coefficient as a gain. You may note that the gain is a conductance times a resistance times a dimensionsless resistance ratio, so overall it has no units. That makes sense, this gain turns a voltage into a voltage. You might also note that gain could be bigger than one: only one of these terms is guaranteed to be smaller than one. In practice in this class, the parallel resistance will usually be a few kiloohms, and gm will be a few milliSiemens, leading to gains ranging from 10 to 200. Finally, you might note that this gain is negative. This indicates that a small increase in base voltage will result in a small decrease in collector voltage from the bias point. This makes sense because the total signal vC=VCC-iC*RC, and iC increases when vBE increases. So our total signal collector voltage goes down when the base voltage is increased, and that's reflected by the negative collector voltage in our small signal model.

Summary

- Transistors can be used to create a small signal voltage gain.
- This amplifier is called a common emitter b/c the emitter is grounded.
- The collector voltage moves opposite the base voltage, resulting in negative gain and current flowing up from small signal ground.
- This negative flow makes sense when small signals are superimposed on the large signal circuit because the total $v_C = V_{CC} - i_C R_C$

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The Generic Amplifier Model

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In this video we're going to make a model that lets us divide the gain we calculated in our last video into a few separate effects, and we'll then latch onto those effects to define design specifications that we can apply to all amplifiers.

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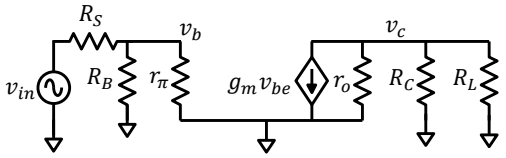
Amplifiers Equations Linked to Source/Load

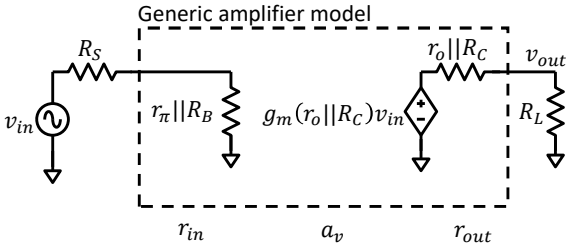


$$v_c = -g_m\,(r_o||R_C||R_L)\frac{r_\pi||R_B}{R_S + r_\pi||R_B}v_{in}$$

$$v_c = -g_m\frac{(r_o||R_C)R_L}{r_o||R_C + R_L}\frac{r_\pi||R_B}{R_S + r_\pi||R_B}v_{in}$$

$$v_c = -g_m(r_o||R_C)\frac{R_L}{r_o||R_C + R_L}\frac{r_\pi||R_B}{R_S + r_\pi||R_B}v_{in}$$

Generic amplifier model



$$v_{out} = \frac{r_{in}}{R_S + r_{in}}a_v\frac{R_L}{r_{out} + R_L}v_{in}$$

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OK, we calculated a relationship between small signal vc, our amplifier's output, and vin in the last video. I've copied the small signal model we used to do that calculation and our final result on this slide. This gain depends on the source impedance driving the amplifier and the load impedance the amplifier drives. That seems a bit weird, we'd like to be able to design amplifiers that work for any combination of sources and loads. One thing that stands out is that there is a voltage divider in this expression, and that the divider is between some resistors that are legitimately part of our amplifier and the source resistance.

CLICK We can expand this parallel combination a little bit

CLICK and then factor out on term to find a second voltage divider embedded in this expression. This one is between the load resistance and some other parameters that are internal to the amplifier. So we can summarize this expression for gain as a voltage gain multiplied by both an output division term and an input division term.

CLICK This format suggests a model for an amplifier where we represent the input by some impedance that divides with the source, and we represent the output as a Thevenin equivalent: a dependent voltage source that captures the amplifier's gain, and a resistance that divides with the load.

CLICK These three parts of our generic amplifier model have names. The first resistor is called the input resistance or rin. Note that we're using small signal notation to denote rin, which is a reminder that this generic amplifier model is for calculating small signal gains. The second resistor is called the output resistance, or rout. Finally, the dependent source is called the small signal voltage gain or av.

CLICK For any resistor, the overall gain is given by a divider between the source and the input resistance, a divider between the source and the output resistance, and the unloaded voltage gain of the system.

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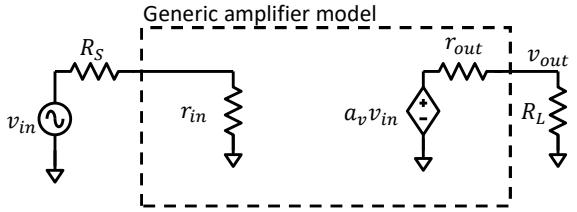
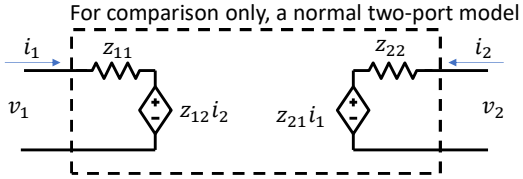
Amp Model is a Two-Port Small-Signal Model



$$\frac{1}{r_{in}} \overset{\text{def}}{\equiv} \frac{\partial i_{IN}}{\partial v_{in}}\Big|_{V_B, R_L, R_S=0}$$

$$\frac{1}{r_{out}} \overset{\text{def}}{\equiv} \frac{\partial i_{OUT}}{\partial v_{out}}\Big|_{V_B, R_S, R_L=\infty, v_{in}=0}$$

$$a_v \overset{\text{def}}{\equiv} \frac{\partial v_{OUT}}{\partial v_{in}}\Big|_{V_B, R_S=0, R_L=\infty}$$



- We presume $z_{12} = 0$, so no feedback to input.
- So we need to take care with R_L and R_S.

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This generic amplifier model is a bit of an extension of models that we've already seen. It clearly has some properties in common with small signal models because we made it out of a small signal expression. It also seems to be informed by Thevenin modeling because this output circuit looks like a Thevenin equivalent. However, this model has two ports, which means that we have extended our previous models, which only considered circuits with one port. Because of that, it's worth formalizing how we calculate rin, rout and av. Doing so will also allow us to think about how we might measure these properties in lab.

CLICK We define rin as the inverse of the change in input current with respect to input voltage. There are a lot of conditions that we want to be true when we evaluate this derivative. The first is just that we want our circuit operating at its bias point when we find rin, and that's because rin is a small signal quantity that depends on the bias point. Second, we want to make sure we have the output loaded with a load resistor that represents a normal load for this amplifier. Though our model doesn't suggest that RL can affect rin, rout or av, we're cutting some corners in modeling that makes having the right RL here quite important for measuring amplifier properties. More on this at the end of the slide. Finally, we want RS to be zero when taking this measurement so that we're only measuring rin. That's a nice ideal, but in practice, we're probably going to add some series RS to use as a sense resistor because measuring voltages is easier than measuring currents.

CLICK rout is similar to rin. We define the inverse of rout as the change in total signal iOUT with respect to small signal variations in vout. As with rin, there are a wealth of conditions on this definition: we have to be operating at the bias point, we need to have a “correct” source resistance, and we’d like RL to be infinity so that it doesn’t fall in parallel with our output resistance. We have one additional constraint when measuring rout, which is that we don’t want our voltage gain to interfere with our measurement – if av*vin is moving around then we won’t know the voltage across rout to measure it – so we make sure the input is _small-signal_ grounded. Note that this doesn’t mean we can hook a wire from our input to ground because that will mess up our bias point. We usually accomplish this small signal grounding by making sure vin is set to zero, i.e.: not generating any signal.

CLICK Finally, voltage gain is defined as the amount of fluctuation in vout when vin varies a small amount. This measurement needs to be taken at the bias point, and when RS is zero, so there’s no input voltage division, and RL is infinity, so there’s no output voltage division.

CLICK This is a great set of parameters that will describe our amplifiers really well. However, it looks pretty different from standard two-port networks. I’ve included one example of a standard two-port network at the bottom of this slide. This is called a Z-parameter network, and it’s only on representation of many that can describe two ports. However, I don’t want to go too far down the rabbit hole of two ports right now, instead I just want to point out that the z12 generator is one major difference between our amplifier model and a standard two port. This z parameter model assumes port 2 can affect the port 1, while our model doesn’t have any element that lets vout influence vin. This is an approximation that holds well for some amplifiers and poorly for others. However, we can paper over omitting feedback in our model by making sure our source and load resistors are correct when we test rin and rout. Doing that means any effect the output has on the input when we measure rin is the same that we would see in operation.

Summary

- We can decouple amplifier behavior from sources and loads with the generic (Thevenin) amplifier model, consisting of r_{in}, r_{out}, and a_v.

- The generic amplifier model is a two-port small signal model, so we defined conditions to measure / analyze r_{in}, r_{out}, and a_v.

$$\frac{1}{r_{in}} \stackrel{\text{def}}{\equiv} \frac{\partial i_{IN}}{\partial v_{in}}\Big|_{V_B,R_L,R_S=0}$$

$$\frac{1}{r_{out}} \stackrel{\text{def}}{\equiv} \frac{\partial i_{OUT}}{\partial v_{out}}\Big|_{V_B,R_S,R_L=\infty,v_{in}=0}$$

$$a_v \stackrel{\text{def}}{\equiv} \frac{\partial v_{OUT}}{\partial v_{in}}\Big|_{V_B,R_S=0,R_L=\infty}$$

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Amplifier Parameters of a Common Emitter Amplifier

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In this video we're going to apply our new amplifier model to the common emitter amplifier. This will give us expressions for rin, rout and av that we can use in a variety of situations. We're going to make one really important decision about our biasing network when we derive these expressions that will help us to generalize to a wide variety of bias circuits.

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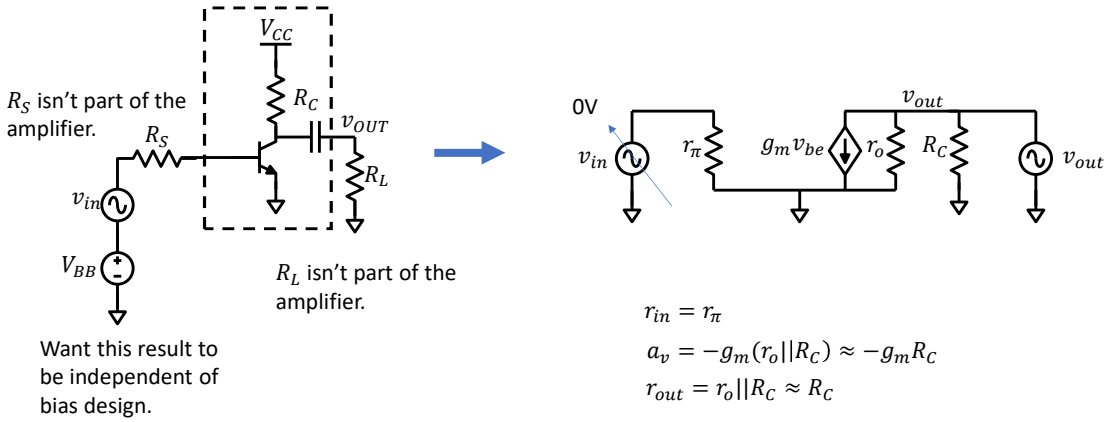
Parameters for a Common Emitter



$r_{in} = r_\pi$

$a_v = -g_m(r_o||R_C) \approx -g_m R_C$

$r_{out} = r_o||R_C \approx R_C$

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I've drawn a common emitter amplifier on the left of this slide, and it's the circuit we're going to analyze to find resuable equations for our common emitter amplifier parameters.

CLICK We've made a few decisions in this circuit that are interesting. First, I've drawn this box around the the amplifier to indicate the boundary of what we consider the amplifier and what we consider the rest of the world. We're trying to analyze the amplifier's properties separately from the rest of the world to which it's connected. That means we'll be zeroing the source resistance when we calculate rin and av, and we'll be opening the load resistance when we calculate rout and av. As a result, I've skipped drawing RS and RL in our small signal model because they don't happen to matter for this analysis. In general though, it's best to draw separate models for calculating rin, rout and av with proper RS and RL values, and I'll comment on why RS and RL don't affect our expressions as I analyze this circuit.

Second, we've picked a very silly set of voltage sources to bias our circuit. This type of biasing is both touch to implement in lab and unreliable, but we will do it for our amplifier analysis because it means that our biasing voltage sources become invisible when we do small signal analysis. This choice of bias lets us analyze our amplifier's properties independent of our network of biasing resistors, and we'll see that modifying the expressions we'll derive to match any particular bias network is usually just a matter of

combining a few resistors in series or parallel.

I'd like you to pause the video and use the small signal model to try to calculate rin, rout and av of the common emitter amplifier.

CLICK From the small signal model, we can see that small changes in vin are applied directly across rpi, so our ratio of input voltage to input current is just given by rpi. When we're finding rin, we assume RS is zero, so it wouldn't affect this calculation. Technically RL was in parallel with RC while we found this value, but common emitters are nice because the output isn't coupled to the input at all, and RL doesn't affect this expression.
CLICK The voltage at the output node is given by the current in the dependent source driven through the resistors at the output, which looks like a parallel combination of ro and RC. This means the voltage is –gm*vbe*ro||RC, and we can note that vbe is equal to vin to observe the gain is –gm*(ro||RC). ro is often much bigger than RC, so it's common to use –gm*RC to describe the common emitter voltage gain in practice. We assume RS is zero and RL is infinity when we find voltage gain, so this small signal circuit is perfectly accurate to our analysis as drawn.
CLICK Finally, we shut off vin and add a stimulus at vout to find rout. The gm*vbe source is forced ot zero current by having zero input voltage, so the output source just sees ro in parallel with RC. Technically we should have included RS in this analysis, but it would just be connected from the base to ground, which wouldn't change what vou see.

Summary

- We derive amplifier parameters for common amplifiers with no bias network. Adapt these expressions as needed to account for biasing.

- Common emitter amplifier parameters:

$$r_{in} = r_\pi$$
$$a_v = g_m(r_o||R_C) \approx g_m R_C$$
$$r_{out} = r_o||R_C \approx R_C$$

- The input is small signal grounded (and not large signal grounded) to measure r_{out}.

In this video we're going to talk about some practical considerations for setting the bias point of common emitter amplifiers. By the end of the video we're going to identify a flexible and robust biasing technique that will see us through most of the class.

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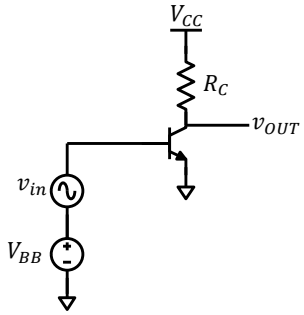
Voltage Source Biasing – Need Precise Bias



- I_C exponentially sensitive to V_{BB}
- Need to stack v_{in} on V_{BB}

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The most naïve way to bias a common emitter amplifier is just to attach a voltage source directly to the base. The only way to add a small signal input to this arrangement is to stack it on top of the biasing source, which is kind of impractical in lab, but you could make it happen if you had to. However, the real issue with this biasing technique is that your bias point is exponentially sensitive to the value of VBB, which is quite impractical for a variety of reasons. It would be hard to make this circuit work reliably.

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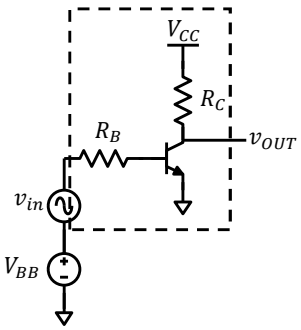
Base R Biasing – β sensitive, Need Stacked V_{in}



$r_{in} = R_B + r_\pi$

$a_v = -g_m R_C \frac{r_\pi}{R_B + r_\pi}$

- $I_B = (V_{BB} - V_{BEON})/R_B$
- $I_C = \beta I_B$
- β varies with temperature and current level, so bias is unstable
- Need to stack v_{in} on V_{BB}

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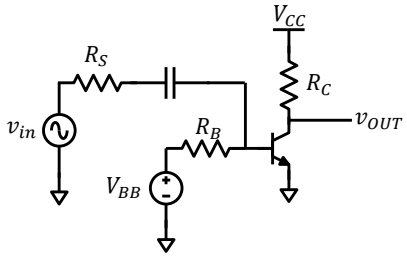
OK, so we can address the exponential dependence on VBB by adding a series resistor in line with the base, which is the circuit we've been looking at for the past two lectures. We can calculate IB easily based on the voltage difference across RB, and then we can use beta to find IC. However, using beta to define your bias point is also fraught. Beta varies with the current level in your circuit and also with the temperature in the room, so your bias point will be unstable in this configuration. Also, we haven't fixed having stacked voltage sources yet.

CLICK This circuit is also a useful example of how to modify the common emitter amplifier property equations to account for your biasing network. If we draw our amplifier border to include RB, then our input impedance will increase to RB+rpi because of the increased resistance in series with the source, but your voltage gain will be reduced by the voltage divider between RB and rpi, which shrinks vbe. Some people think adding base resistance is a free lunch when you need to boost your rin, but you pay for it with gain. rout is unchanged by the addition of the base resistance, and that's usually true when accounting for bias networks.

… appears to increase rin, but it costs av to do so
… generally should include bias network in your input impedance because sources see it. We'll have lots of HW problems to that effect.

Base R w/ AC Coupled Input – β, Mid-Band



$r_{in} = r_\pi || R_B$

- Fixes stacked voltage source
- Depends on v_{in} being AC, cap being big enough.
  (The mid-band assumption)
- I_C still fluctuates with β

We can fix our stacked voltage source by using AC coupling to connect a signal to the base at AC and not DC. Whew, that problem was annoying. However, we're still relying on a series base resistor to set our bias point, and so we're still haunted the risk of IC changes as beta moves around.

This variation of the common emitter has a rin of rpi in parallel with beta because the large signal VBB will be grounded, which leaves RB connected from the base to ground. av and rout are unaffected by this bias network.

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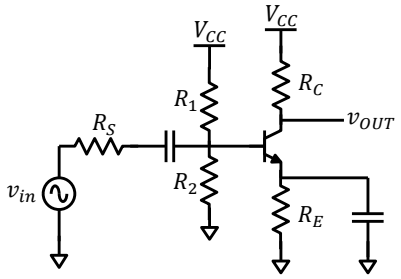
Voltage Divider and Degeneration Resistor



$r_{in} = R_1||R_2||r_\pi$
(R_E doesn't appear b/c shorted)

- Easy to set bias if $\frac{V_{CC}}{R_1+R_2} \gg I_B$

$$V_B \approx \frac{R_2}{R_1+R_2}V_{CC}$$

$$V_E = V_B - V_{BEON} = I_E R_E$$

$$I_C \approx I_E = (V_B - V_{BEON})/R_E$$

- Capacitor in parallel with R_E grounds emitter at AC. (Mid-band assumption again)

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Finally, we come to a biasing solution avoids all the problems we've been complaining about during this video. We AC couple our input to avoid stacking voltage sources, and we are using a new technique to set our collector current. Instead of setting base current and the letting beta determine the collector current, we're going to try to set the base voltage, which lets us calulate the collector current without using beta.

The first step of this process is setting the base voltage, which we do with a voltage divider between R1 and R2. However, the voltage divider equation only works when there is no current pulled out of the middle node of the divider, and the base draws some current. So we have to account for base current in one of two ways when designing this type of bias. One is to make sure there's a lot of current running in R1 and R2 so that the base current is only a small fraction of it, which is how you arrive at the inequality I've specified at the top of the right column. The other is to do an exact calculation for the voltage assuming IB is being pulled out of the central node. That's tedious algebra that you can figure out on your own, and you may have to do so in the next few labs.

Once we know VB, we know that VE is just a diode drop below the base, so VE=VE-VBEON. VE also has to be equal to IE*RE, and IE is about the same as IC. So by picking R1, R2 and RE, we can set IC independent of beta. Just as long as beta is big, we'll have a known bias point.

However, our small signal analysis of the common emitter depended on the emitter being grounded. We make that true for our small signal circuit by putting a big capacitor in parallel with RE that will short the emitter to ground at high frequencies. This works well, but it means our amplifier will only work for a certain range of frequencies – frequencies that are high enough to short all the caps we care about, while being low enough that parasitic caps don't mess up our measurement. The range of frequencies for which those two conditions are true is called the mid-band, so the operation of this common emitter relies on the mid-band assumption. We were already using the mid-band assumption to AC couple our input signal, so there's little harm in relying on it to ground our common emitter too.

The input resistance of this circuit is given by R1||R2||rpi because VCC is shorted in a small signal model, which means both R1 and R2 hang from the base to ground. RE doesn't appear in this expression because we presume our small signals are high-frequency, so RE is shorted out and the emitter is grounded in the small signal analysis of this amplifier. You may notice that a desire to have a big rin is in tension with the desire to have very high current in R1 and R2. That's a drawback of this style of biasing.