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Review of Linear Circuits & Dynamics

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E151 – Analog Circuit Design

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In this video series we're going to be reviewing linear circuit theory. We'll also think carefully about how linear circuit theory relates to matrix and graphical representations of linear systems, and that will help us come up with some very quick ways to solve circuits. This practice of relating circuits to mathematical concepts is one of the recurring habits of mind that shows up in this course, so watch out for it!

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Matrix Model of Circuit Linearity

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In this video we're going to review how to solve linear circuits and we'll relate those techniques to a matrix representation of a linear circuit.

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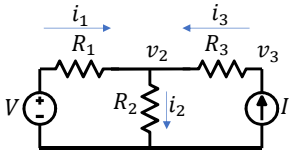
Find i2 in 3 Ways



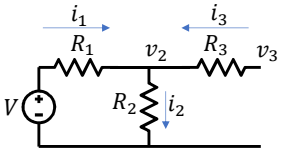
KVL

$$V = i_1R_1 + i_2R_2$$
$$= (i_2 - I)R_1 + i_2R_2$$
$$i_2 = \frac{V + IR_1}{R_1 + R_2}$$

KCL

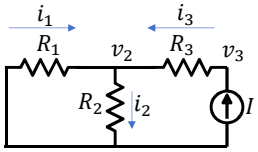
$$i_2 = \frac{V - v_2}{R_1} + I$$
$$R_1 i_2 = V - i_2R_2 + IR_1$$
$$i_2 = \frac{V + IR_1}{R_1 + R_2}$$

Superposition



$$i_{2V} = \frac{V}{R_1 + R_2}$$

+



$$i_{2V} = \frac{R_1}{R_1 + R_2} I$$

$$i_2 = \frac{V + IR_1}{R_1 + R_2}$$

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We're going to start off with an exercise. Pause the video and try to calculate i2 for this circuit in three different ways.

One way uses Kirchoff's voltage law, abbreviated KVL, as a starting point. There are several variations on this theme, but we can imagine drawing a KVL loop around the left mesh of this circuit to find our first equation: V=i1R1+i2R2. CLICK Then we can use Kirchoff's current law, abbreviated KCL, to express i1 in terms of i2 and I because those three currents add together at node v2. CLICK Finally, we do some algebra to arrive at a solution.

Another way uses Kirchoff's current law as a starting point. We write the currents adding together at node v2 in terms of the voltages on adjacent nodes, which gives us an equation in two unknowns right away. CLICK Then we can rearrange that eqatuion by cross multiplying R1 CLICK and finally arrive at the same answer that we found using KVL.

The third way I thought of was using superposition, which is a technique that always seemed a little magical to me. We draw two superposition subcircuits, calculate i2 in each of them, then add the superposition subcurrents to find the final value of i2. As a reminder, we drew the superposition subcircuits by "zeroing out" all but one power source in each subcircuit, where zeroing voltage sources looks like shorting them (setting V=0, like a wire) and shutting off current sources looks like opening them (setting I=0, like an open

circuit). This is a super slick technique that lets you solve circuits very quickly because the superposition subcircuits are often very simple.

This technique of drawing multiple circuits to represent some mathematical manipulation is a common tool that we'll come back to often in this class. We do this because it lets us calculate quickly by simplifying circuits so we can analyze them in our heads. Keep an eye out for it!

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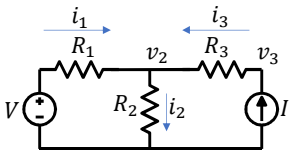
Circuits Can Be Represented as Matrices



$$\begin{bmatrix} V \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} R_1 & R_2 & \\ & R_2 & \\ & R_2 & R_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ I \end{bmatrix}$$

$$\begin{bmatrix} V \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} R_1 \\ \\ \end{bmatrix} i_1 + R_2 i_2 + \begin{bmatrix} \\ \\ R_3 \end{bmatrix} I$$

- Each superposition circuit represents a set of vectors and/or submatrices you can add back together to get a solution.

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The magic of superposition can be explained by looking closely at the matrix representation of a linear circuit. On this slide I've drawn a matrix equation that summarizes all of the voltage-current relationships enforced in the circuit. You can see an example by multiplying the first row by the input vector, which results in the equation V=i1R1+i2R2, our first KVL loop from the last slide. There's a lot of depth in this representation that we're only going to glance at – for instance, the matrix is actually an adjacency graph which shows how much resistance is connected between different nodes – CLICK but we are going to do one quick manipulation to help justify superposition without fully proving it. This second representation shows that the current source I controls just one vector term in a matrix equation, and because that equation is linear, you could imagine calculating the contribution of the other two vectors with I set to zero, then adding in the effect of the I vector. That ability to analyze terms of a linear equation separately is at the heart of superposition.

Aside: there are many different formulations of this circuit matrix, which each correspond to different circuit solving techniques.

Summary

- You can solve circuits with KVL, KCL or superposition
- "Zero Out" supplies in to make superposition subcircuits
  - Current source becomes open (i.e. I=0)
  - Voltage source becomes short (i.e. V=0)
- Superposition subcircuits correspond to subsets of the matrix representation of a circuit.

In this video we're going to review finding Thevenin equivalent circuits. We'll also relate finding Thevenin circuits to a graphical representation of current-voltage relationships called, creatively, an IV plot.

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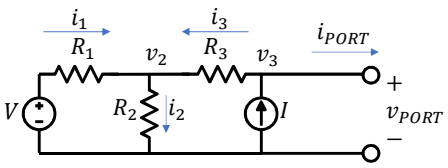
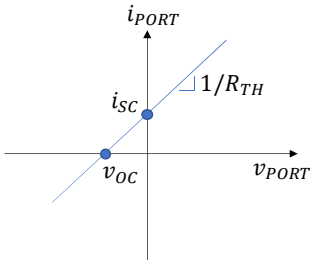
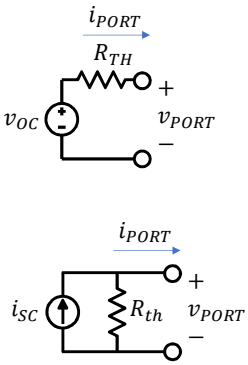
Thevenin Lets Us Analyze Circuit Connections







$$i_{PORT} = i_{SC} + v_{PORT} \cdot 1/R_{th}$$

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I've brought the circuit we analyzed in the previous video over to this slide. We are now very capable of solving the circuit, finding every voltage and current in it, either using matrix math or standard node-by-node circuit analysis techniques, but just knowing what's going on inside of a circuit is a little uninteresting. Ultimately, we're going to want this circuit to interact with the rest of the world, either by hooking it to another circuit or to some transducer that cares about the voltage and current it provides. CLICK We represent this connection to the rest of the world using a port.

CLICK We'd like to abstract away the details of this circuit, and we can take advantage of the fact we connect at a port to do so. If we can describe the relationship of port voltage to port current, then whatever we're connecting to the circuit can just use the port I-V relationship instead of representing the whole circuit. This graph does so, and we know that a simple line on the iPORT-vPORT plane suffices to describe the circuit because every element in it is linear. When we change vPORT, iPORT has to change in a linear way because there's no element that would cause it to change in any other shape.

I've labeled a few details of this IV plot. The x-intercept is called the open-circuit voltage and labeled vOC. This is because open circuits have no current running through them, so if you connected an open circuit to the port you would have a port current of zero and a port current of the x-intercept. The y-intercept is called the short circuit current and labeled iSC.

This is because short circuits have zero voltage across them, so if you connected a short across the port terminals you would have a port voltage of zero volts and a port current of the y-intercept. The slope of the line is named after a special resistance called the Thevenin resistance. The slope is labeled as 1/RTH because the rise-over-run on this plot would have units of amps-per-volt, which is the inverse of resistance.

CLICK We can represent this linear graph using some equivalent circuits, either the Thevenin equivalent (pictured on top) or the Norton equivalent pictured on the bottom. I think it is particularly clear how the Norton equivalent relates to the graph because it directly implements the slope-intercept form of the IV relation for the port.

I'd like you to pause the video and find the Thevenin resistance for this circuit in two different ways.

CLICK One way is to very directly find the rise and run of the line on the previous page. Two convenient points to use for a rise-over-run eqauation are Isc and vOC, which I calculated here using superposition. Calculating their ratio turns into some messy math for this symbolic representation, so I didn't follow it through. However, this calculation technique can be very useful when you have measured values of iSC and vOC.

(As a side note, though you'll do a lot of algebra in learning analog design, I'm trusting you as learners to go through the steps by yourself when you need to. I'll vary the level of detail I show to try to highlight important concepts or common circuit solving techniques. You should always feel free to pause the video and work algebra out for yourself.)

CLICK A much faster way is zeroing out all of the sources in the circuit and then calculating the equivalent resistance seen by the port. I've drawn a copy of the circuit with the sources zeroes, which makes the current source open and the voltage source short, and calculated the equivalent resistance. This algorithm can seem as magical as superposition, but the reasoning behind it is anchored in the linear IV curve we just looked saw. CLICK This curve can be reduced to a slope-intercept equation, but we can trace the existence of the

intercept to the power sources I the circuit. The power sources must create the intercept because resistors have zero current when zero voltage is applied. So when we zeroing the power sources in the circuit we eliminate the intercept, which lets us calculate the slope directly from the remaining resistors.

One quick definition: IV curves where the curve passes through zero and only exists in quadrants 1 and 3, like resistor networks, are called passive. They're called passive because they can't generate power at the port, which can happen when the curve passes through quadrants 2 and 4.

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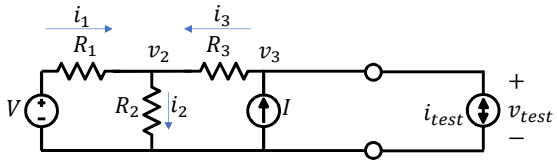
Test Sources Also Let You Find R_{TH}



- Apply a small test signal and resulting small signal port behavior
  - eg: apply i_{test} and calculate v_{test}
  - OR: apply v_{test} and calculate i_{tes}

  } Decision can simplify math
- Shut off supplies because they don't experience differential changes
- Identical to calculating R_{TH} for simple linear networks, helpful later.

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There is one other way to calculate Thevenin resistance that you may not have been explicitly taught, which is applying a test source. As a preview of how this method works, the mathematical analog to solving a circuit with a test source is taking a derivative of the IV curve. Keep that in mind as we discuss them.

Test sources are differentially small sources that you attach to a port. You apply a differential signal to a port, either a voltage or a current, using the source, which sets one of your two port variables. You then calculate the other variable, for example finding vPORT if you apply a test iPORT, and use that second variable to find RTH by taking the ratio it with your test variable.

When you do this analysis, you need to shut off supplies because they don't undergo differential changes. It doesn't matter if the values in a circuit underwent a tiny change: a votlage source will still have V across it and a current source will still have I through it. I often pithily summarize this behavior as "voltage sources are where little wiggles go to die."

You may notice that shutting off supplies and calculating the voltage produced by a test current is identical to the slope-intercept method we talked about on the last page. That's true for resistor networks, but this technique will prove useful later. Another thing that will

prove useful later is the freedom to choose whether we're applying a vTEST or an iTEST, sometimes on test source makes the math much easier than the other.

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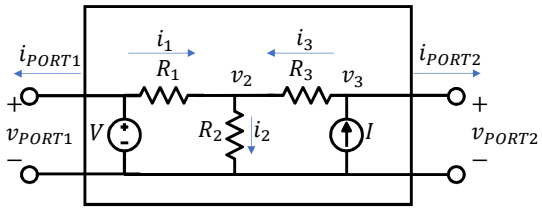
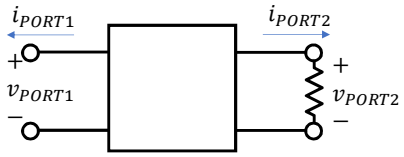
A Note on Two-Port Networks

- What types of devices have two ports?
  - Coaxial cables
  - Resistor dividers
  - Amplifiers
  - Transformers



- Rich and interesting theory of modeling two-ports as matrices
  - Don't have R_{TH}!
  - Requires the network to be linear and passive
  - In general, port 1 can affect port 2 AND vice versa
- Terminating port 2 makes 2 ports into 1 ports:



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Thevenin resistances and open circuit voltages are great ways to represent circuits with one port, but there are a lot of circuit elements in the world that have two ports. I'd like you to pause the video and see if you can write down a few two port circuits. As a hint, think about circuits that either have an input and an output, or which have two ends.

CLICK Some of the examples I came up with include coaxial cables, resistor dividers, amplifiers, transformers, and this crazy mutation of the circuit we've been looking at which has a second port bolted on to it. The box I've drawn around the circuit indicates what the two port abstraction is trying to hide from the world: rather than having us worry about the guts of this circuit, the two port abstraction tries to just summarize how each port affects the other.

CLICK There are a lot of interesting things I could say about two ports, but we're going to skip almost all of them in this class. RF delves into this topic much more deeply. One detail that's worth mentioning is that two ports don't have just one Rth because two ports describe the relation among four variables – vPORT1, iPORT1, vPORT2 and iPORT2 – which requires more numbers to summarize. Another is that the two-port I've drawn wouldn't actually play well with two port theory because theory demands that two ports be linear, which this is, and also passive, which this is not. Finally, it's really important to take away that port1 can affect port2 AND port2 can affect port one, which is a property called

bilaterality. So even if you're only measuring port 1, things that are connected to port 2 can change your measurement.

CLICK That last detail is so important because the trick we're going to use to bypass two-port analysis is terminating the second port of our two port networks. That makes them into one-ports – only vPORT1 and iPORT1 could get hooked up to the outside world in this example – but bilaterality means that a bad choice of termination resistor can change our measurements or analysis. Put a pin in that idea for when we start measuring amplifiers.

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Dependent Sources

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In this video we're going to introduce some circuit elements called dependent sources.

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What's a Dependent Source?

$i = g_m v_{CONTROL}$

$v = k v_{CONTROL}$

- Current or voltage is set by value somewhere else in the circuit, not across the terminals.
- Can't eliminate with superposition in all cases, analyze w/ test source.

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Dependent sources are circuit elements that have a fixed voltage or current that is determined by a voltage that is not applied across their terminals. I've drawn two examples on this slide, a voltage controlled current source that has a value of gm times some control voltage. gm is the transconductance of the dependent source, and the word transconductance is a terrible portmanteau of transfer and conductance. Old-timey electrical engineers really liked terrible portmanteaus, but they were usually talking some sense: in this case, gm has units of conductance because it turns a voltage into a current, and it transfers the effect of that voltage somewhere else in a circuit.

I've also drawn a voltage-controlled-voltage-source on this slide. I've drawn it's governing equation next to it. Current-controlled-voltage-sources and current-controlled-current-sources area also things that can exist, and they would be described by different governing equations, which are usually included next to the element on a schematic.

Dependent sources introduce some tricky problems into our other analysis techniques because they can create unusual dependencies in our circuit matrix. As a result, it's not always safe to remove them with superposition. They're also neither resistors nor power sources, so our techniques that rely on equivalent resistances don't work well with dependent sources. As a result, the only surefire way to analyze a circuit with a dependent source is to apply a test source to it.

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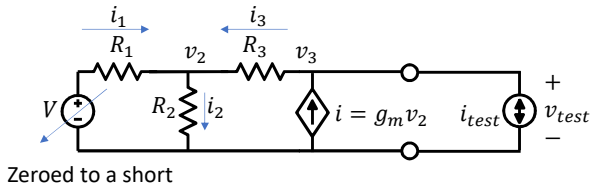
You Need to Use Test Sources to Find R_{TH}



$$i_2 = \frac{v_2}{R_2} = \frac{R_1}{R_1 + R_2}(i_{test} + g_m v_2)$$

$$v_2\left(1 - \frac{R_1 R_2}{R_1 + R_2}\right) = \frac{R_1 R_2}{R_1 + R_2} i_{test}$$

$$v_2 = \frac{(R_1||R_2)}{1 - g_m(R_1||R_2)} i_{test}$$

$$v_{test} = \left(R_3 + (R_1||R_2)\right)\left(1 + \frac{g_m(R_1||R_2)}{1 - g_m(R_1||R_2)}\right) i_{test}$$

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Here's an example of doing just that.

I've chosen to apply a test current source to this circuit because it is in parallel with the dependent source and I can add their currents together. That makes the math easier than if I'd chosen a test voltage source.

CLICK, I start calculating the behavior of this circuit by finding the value of v2, which will let me write much simpler expressions for the test current source. Trying to isolate the control variable is usually a good plan when analyzing circuits with dependent sources. I do this by noticing that all the current from the parallel test and dependent sources will flow through R3, then it will split between R1 and R2 according to a current divider. If I cheekily write i2 as v2/R2, I can find an equation that is only in terms of v2.

CLICK You can rearrange this equation by cross multiplying the R2 and then gathering terms.

CLICK and finally you can express v2 in terms of itest. I've simplified this expression by writing R1R2/(R1+R2) as R1||R2.

CLICK Using that expression, we can write the total current flowing out of our parallel

current sources as a coefficient multiplied by itest. That total current gets driven into the resistor network, which has an equivalent resistance of R3+R1||R2. That resistance times the current gives us vtest. vtest/itest is RTH, and it would be simple to divide itest off of this expression to reveal that the coefficients on the right hand side are the RTH for this network.

This RTH is a bit weird! Most notably because there are values of resistance and transconductance for which it is infinite! That corresponds to the case where raising vtest causes the current flowing through R3 to exactly match the externally applied voltage, so there was never a current difference across R3 to pull down any itest. This kind of situation can occur because the dependent source represents a kind of feedback in a circuit, and feedback can have surprising consequences including instability. So be wary whenever you see a dependent source.
A form of Feedback …

Summary

- Dependent sources have their voltage or current set by a control voltage or current somewhere other than their terminals.
- Analyze dependent sources with test sources.
- Dependent sources can do weird stuff!

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Step Responses in Circuits: Initial and Final Value Theorems

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E151 – Analog Circuit Design

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In this video we're going to learn or review a few theorems related to the Laplace transform to find very fast ways to analyze dynamics in circuits.

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We're Revisiting Dynamics to Solve Steps Fast

- Common circuit inputs
  - Sine → find a transfer function using impedance
  - Step → Inverse Laplace? Pattern Match? Solve a DE?
- Some tactical advantages that will help us solve for steps faster
  - most circuits are 1st order
  - impedance makes it easy to find transfer functions
- Aside, there are other common inputs:
  - Ramp: Ignore the startup behavior, then it's kind of a DC problem
  - Exponential rise, like $\left(1 - e^{-t/\tau}\right)$: Approximate as a ramp

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To start this process, I'd like you to pause the video and try to write down the most common shapes for waveforms that are applied to circuits.

CLICK The two that sprang to my mind are sine inputs, which are easy to analyze using transfer functions or Bode plots, and step inputs, which require some more involved math. We could try an inverse Laplace transform or a differential equation, but those aren't really fast enough to use in a lab. Or we could lean on pattern matching in some cases, but circuits tend to present lots of variations on a theme that make pattern matching difficult.

CLICK We're going to take advantage of a few facts about circuits in this class to come up with easy approaches. First, most amplifier circuits can be approximated as first order, which simplifies the types of waveforms we'd expect. Second, impedance makes it very easy to find transfer functions. So if we can use transfer functions to quickly identify the distinguishing features of a first order circuit – the starting value, ending value and time constant – then we can easily describe our step responses.

CLICK We'll start that in just a second, but there are a few other circuit inputs I want to mention first. Ramp inputs have a DC character, where all of your slopes are constant, after overcoming a weird initial transition. You can often analyze them using pseudo-DC time domain methods. Exponential rise times are common in circuits because almost

everything in nature is some kind of low-pass filter. Depending on your needs, you can often approximate these as funny looking ramp inputs.

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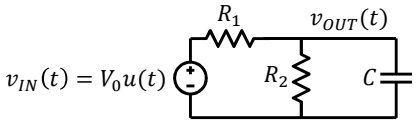
Step Responses from Transfer Functions



$$\frac{v_{OUT}(s)}{v_{IN}(s)} = \frac{(\frac{1}{Cs}||R_2)}{R_1 + (\frac{1}{Cs}||R_2)}$$

$$\frac{v_{OUT}(s)}{v_{IN}(s)} = \underbrace{\frac{R_2}{R_1 + R_2}}_{\text{DC gain}} \cdot \underbrace{\frac{1}{(R_1||R_2)Cs + 1}}_{\text{Time constant, } \tau}$$

General Theorems

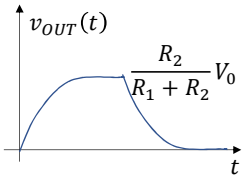
Final value theorem: $\lim_{t\to\infty} f(t) = \lim_{s\to 0} sF(s)$

Initial value theorem: $\lim_{t\to 0} f(t) = \lim_{s\to\infty} sF(s)$

For our Example

$$\lim_{s\to 0} sv_{OUT}(s) = \lim_{s\to 0} s\frac{v_{OUT}(s)}{v_{IN}(s)}\frac{V_0}{s} = \frac{R_2}{R_1 + R_2}V_0$$

$$\lim_{s\to\infty} sv_{OUT}(s) = \lim_{s\to\infty} s\frac{v_{OUT}(s)}{v_{IN}(s)}\frac{V_0}{s} = 0$$



A falling edge would be $V_0(1 - u(t))$, so use linearity and add response to V_0 to response to $-V_0 u(t)$

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Focusing back in, we'd like to find the initial value, final value, and time constant of the step response that this first order circuit will have in response to the step input. We know the response will be first order because there is only one energy storage element in the circuit, the capacitor, so there can't be more than one power of s running around in our Laplace transform.

We can start doing that by finding our transfer function and putting it into factor form. CLICK we find our transfer function using an impedance divider, where the parallel combination of R2 and C is divided against R1. CLICK Some only modestly tedious algebra will reveal this factor form, which I think is beautiful for a few reasons. One is that the time constant is immediately visible in factor form because the denominator must be of the form tau*s+1. Another is that factor form does a really good job of separating out DC behavior of a circuit, what it would do if signals weren't changing, from dynamic behavior of a circuit, what happens in response to changing inputs. For example, if this circuit were driven by a constant voltage, we could ignore the capacitor and the circuit would just behave like a resistor divider. The DC term is just a resistor divider equation, which captures that behavior. I think the factor form lends a lot of insight into the behavior of a dynamic system, and I encourage you to write your transfer functions in factor form in this class.

CLICK Next we're going to find our initial and final values using the initial and final value theorems, which I've included here. These theorems relate the limits of a time domain function to the limits of its Fourier transform times s. One pneumonic I use to remember which is which, is that I think of s as a frequency, and remember that high frequency (or big s) corresponds to small time and vice versa. That helps me recall whether taking s to infinity or zero will give me initial or final values.

CLICK In our example, the function we care about is vOUT(t), which is where we'll see our step response. We know the transfer function from our impedance analysis above, so we'll take the limit of s*vOUT(s) and then write vOUT as the product of the transfer function and the Laplace transform of our input step. One trick when you're evaluating the initial and final value theorems for step inputs is to remember that the input itself, V0/s, cancels with the s that hangs out in front of F(s) by the IVT or FVT. This means that your final value can be found just by letting s go to zero in your transfer function or the initial value can be found by letting s go to infinity in your transfer function (but again, this trick only works for steps). Doing that gives us our initial and final values of 0 and a divided V0.

CLICK, so our waveform is going to be a first order rising shape from zero to a divided V0. I've also included a falling edge on this waveform, which hopefully will look familiar or seem to be common sense to you, but that falling edge doesn't actually line up with the math we've derived thus far. We could just put a negative sign in front of V0 to guess the initial and final values of a negative step response in our system, and that would predict a negative final value, which disagrees with what I've drawn here.

CLICK That's because falling a falling edge of a square wave driving this system would be represented by the equation V0(1-u(t)), not just –V0*u(t). So if you're going to use the initial value theorem, remember that your initial value has to be added to any initial condition the system currently has.

This form separates DC and AC behavior, which is a really good plan.

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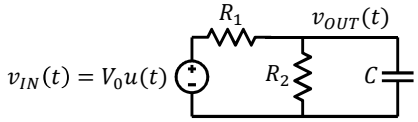
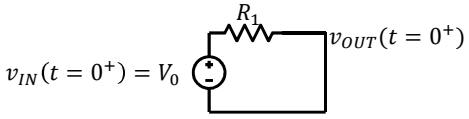
Step Responses from Initial and Final Circuits

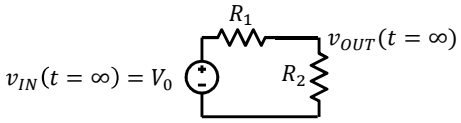


$$\frac{v_{OUT}(s)}{v_{IN}(s)} = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{(R_1 || R_2)Cs + 1}$$

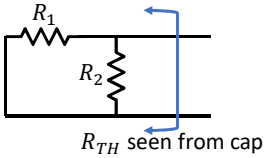
Time constant, τ



$s \to \infty$ when using the IVT, so $1/Cs$ shorts out resistors



$s \to 0$ when using the FVT, so $1/Cs$ is an open circuit



If there's one capacitor, then $\tau = R_{TH}C$ seen from the capacitor
(works for inductors. Can work for 2 "non-interacting" elements)

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The initial and final value theorems are nice, but we can punch them up by realizing that they have circuit interpretations that let us draw simplifying subcircuits. We're going to pursue that technique on this slide, and I've brought our transfer function from the last page so that you can compare our results to those implied by the transfer function.

CLICK When you're applying the initial value theorem, you let s run to infinity. If we did that with our impedances before we found our transfer function, we'd observe that capacitors all have negligibly small impedance compared to resistors. That means you can draw an initial value circuit, also called an AC circuit, where many capacitors are replaced with short circuits. Doing so for our example reveals that the output node is shorted to ground by the capacitor at time 0+, so we know our initial value will be zero.

I hedged my language when describing this technique because you can't always just replace capacitors with shorts. You need to be mindful if there's more than one that capacitor in the circuit because they aren't going to be negligibly small impedance compared to one another. However, capacitors will always short out resistors in initial value circuits.

CLICK We can use a similar technique for the final value theorem that lets us draw a final value, or DC, circuit. In final value circuits, capacitors are replaced by open circuits. This reveals that the final value of vOUT is given by a voltage divider on V0.

CLICK Finally, we need to find our time constant. If a circuit has only one capacitor, then the time constant is going to be given by the capacitance times the Thevenin resistance seen looking out from the capacitor. This makes sense because any charge moves onto or off of the cap through that Thevenin resistance. In this case, we can quicly see the equivalent resistance is R1||R2.

This technique works for single inductors in a circuit as well. It can sometimes work when there are multiple energy storage elements in a circuit, but those elements need to be isolated from one another so that they don't result in a second order transfer function. That kind of isolation either tends to be a lucky case, like two caps that can be merged in parallel, or carefully designed.

Summary

- We can calculate circuit responses to sine inputs with Xfer functions
- We can calculate circuit responses to step inputs two ways
  - Xfer functions with IVT, FVT and pattern matching to find τ
  - Initial and final circuits and Thevenin resistance seen from the cap to find τ

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Examples of Step Responses

Matthew Spencer
Harvey Mudd College
E151 – Analog Circuit Design

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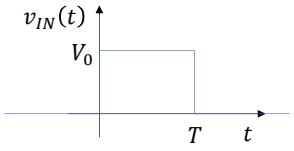
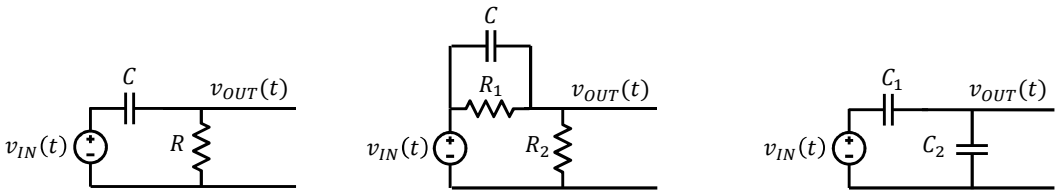
In this video we're going to get some practice with the dynamics tricks we just learned.

Department of Engineering

Try to Draw the Response of These Circuits

$$v_{IN}(t) = V_0(u(t) - u(t-T))$$





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I would like you to pause your video and draw the value of vOUT when the input on the top of this slide is applied to each of the circuits on the bottom. This is a great practice exercise, so I'd really like you to take the time to do it, and maybe compare notes with a friend, before you keep watching. We'll go through the answers when your resume the video.

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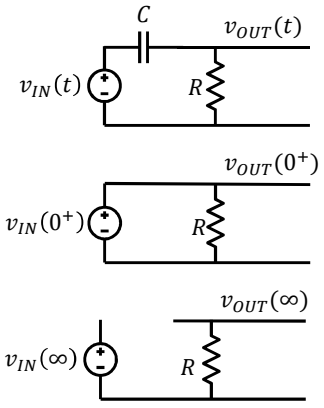
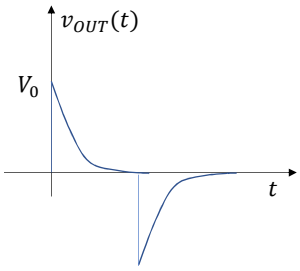
High Pass Filter



$$\frac{v_{OUT}(s)}{v_{IN}(s)} = \frac{R}{R + 1/Cs} = \frac{RCs}{RCs + 1}$$

IVT: V_0, FVT: 0, $\tau = RC$



$\tau = RC$

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The transfer function for this high pass filter can be calculated from an impedance divider, and the initial and final value theorems give us values of V0 and 0 respectively. Pattern matching gives us a time constant of RC.

CLICK That suggests that our step response will rise to a value of V0 at the start and exponentially decay back down to zero. The falling edge will cause the opposite effect.

CLICK We could get there with initial and final value circuits. The initial circuit has vOUT shorted to vIN, so you'll see the full step at first. The final circuit has an open circuit between vOUT and vIN, so vOUT will be pulled to ground by the resistor R. The time constant is RC because the Thevenin resistance seen by the cap is R.

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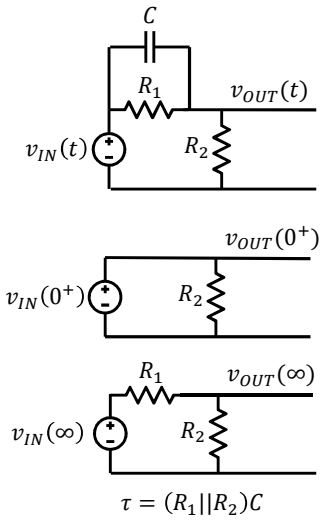
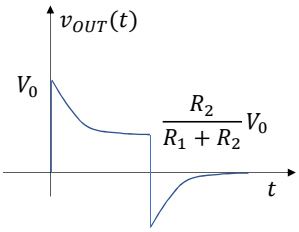
Resistor Divider with Capacitive Feedthrough



$\tau = (R_1||R_2)C$

$$\frac{v_{OUT}(s)}{v_{IN}(s)} = \frac{R_2}{R_1 + R_2}\frac{(R_1||R_2)Cs}{(R_1||R_2)Cs + 1}$$



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We'll take the opposite order of solutions for this resistor divider with capacitive feedthrough because the transfer function is rather involved.

CLICK the initial value circuit shows the input shorted to the output like the high pass filter, so we expect an initial value of V0. The final value circuit shows a voltage divider that set the final value to a divided V0. The Thevenin resistance seen from the cap is R1||R2, so the time constant is (R1||R2)*C.

CLICK This lets us draw the step response, which has a few interesting features. First, the waveform has high initial values after steps that decay down to smaller final values. This behavior is called capacitive feedthrough. Feedthrough happens whenever a capacitive and resistive path are in parallel, and it is also linked to having zeros in the numerator of your transfer function. There are some deep links between Laplace math and circuit design that you can infer from that relationship, keep an eye out for them.

Second, the falling edge of this wave has a negative voltage. On our falling edge, our initial value from the negative step, which is –V0, is added to the final value from our rising edge, which is a divided version of V0. That means we have a brief negative value. Don't forget that the result of the IVT has to be added to the value of the wave right before the step you are analyzing.

CLICK Finally, I reverse engineered the transfer function from the results of my circuits. I knew the DC coefficient had to be a voltage divider, and I knew the denominator of the dynamics term had to be (R1||R2)Cs+1. After I filled those in, I picked a numerator for the dynamics that would result in an initial value of V0.

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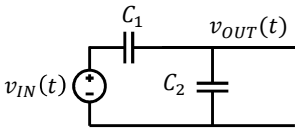
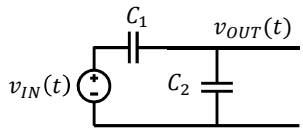
Capacitive Divider

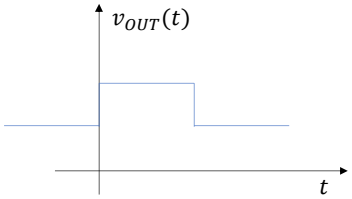


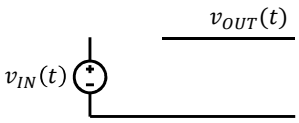
$$\frac{v_{OUT}(s)}{v_{IN}(s)} = \frac{1/C_2 s}{1/C_2 s + 1/C_1 s} = \frac{C_1}{C_1 + C_2}$$

Contains no s, so IVT=FVT=$V_0 C_1/(C_1 + C_2)$



AC circuit same as we started with





DC circuit is missing!
v_{OUT} has an unknown DC value

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Finally, we're left with the capacitive divider, which is a strange duck. It's easy enough to calculate it's transfer function, which doesn't have s in it! That means the transfer function is claiming to have the same behavior for all input frequencies!

CLICK Drawing initial value and final value circuits doesn't help much. The initial value circuit is the same as the circuit we started with. The capacitors won't short each other out, so we need to keep both of them. The final value circuit just reveals that vOUT isn't connected to any DC signals. That means we have an unknown DC value at the output!

CLICK These facts point to the behavior of the ideal capacitive divider, which is that it will faithfully represent a divided version of the input signal at the output, just like an ideal resistor divider. However, if there's a DC value at the output of a capacitive divider, then it will stay there forever because there is no resistor to discharge the output. Weird!

However, even though this seems weird, the behavior is real. One thing to keep in mind is that capacitive dividers can transmit very sharp square waves without rounding their corners, faster even than resistive dividers because small parasitic capacitances attached to circuit output nodes are very common, while small parasitic resistances attached to circuit output nodes are quite rare.

Summary

- Use initial and final circuits to find step responses, it's fast and fun!
- Capacitive feedthrough comes from parallel resistive and capacitive paths to an output
- Ideal capacitive dividers have infinite bandwidth and will hold a DC value forever.