1 Lab Introduction

In this lab you will build amplifiers, measure their frequency and step responses, and compare them to various analytical models The learning goals are listed below:

- See the full frequency response of an amplifier and appreciate its complexity
- Understand how well the Miller approximation and exact models frequency models work
- Extract common parastiics that matter at high frequencies
- Mitigate the Miller effect using a Cascode
- Get practice calculating open circuit time constants

2 Common Emitter Frequency Response

1. Find the row-to-row capacitance of your breadboard.
2. Build two common emitter amplifiers with gains of 120, collector currents of 1mA and supply voltages of 15V. Use the same design for both (i.e.: same R_c, R_e, C_e, etc.), but lay them out on your breadboard differently as shown in Figure 1: one device has its terminals on adjacent rows while the other has the rows between terminals grounded. We will refer to the amplifier with layout A as amplifier A and the amplifier with layout B as amplifier B.
3. Measure a Bode Plot of a_v for each amplifier out to as high a frequency as possible. Try to capture the second order pole and the feed-forward zero.
4. Build analytical models for both amplifier layouts using your values of row-to-row capacitance, information from the datasheet, and the full common emitter transfer function from lecture. C_π and C_μ aren't listed directly on the datasheet (the C_{ibo} and C_{obo} in the table are **not** C_{pi} and C_{mu}), so you'll need to figure out how to extract junction capacitance from datasheet values/graphs, and you'll need to figure out how to calculate base capacitance from datasheet values. Though there may be a path to finding base capacitance from charge storage time, f_T is a great way to find one of C_π or C_μ if you know the other. Consider how the breadboard parasitics interact with C_π and C_μ.
5. Build yet more analytical models for both amplifier layouts using the Miller approximation instead of the exact transfer function.
6. Compare your data and your models by making Bode plots with the sets of data listed below overlaid. Comment on the accuracy of the models and the difference between the layouts.
   (a) measured data from amplifier A and measured data from amplifier B
   (b) measured data from amplifier A, full transfer function model of amplifier A, and Miller model of amplifier A
   (c) measured data from amplifier B, full transfer function model of amplifier B, and Miller model of amplifier B
7. Measure the step responses of both amplifiers and explain their features (time constants, initial values, etc.) using your analytical models. How can you measure a step response when your input is AC coupled? Does the amplifier step response appear to be first or second order? Does the feed-forward zero appear in the step response?
8. Measure r_{in}, r_{out} and V_{SW} of amplifier B.

Required Data: row-to-row capacitance, designs for your amplifiers, Bode plots listed above, one paragraph of discussion for each Bode plot, step response traces, answers to questions about step response

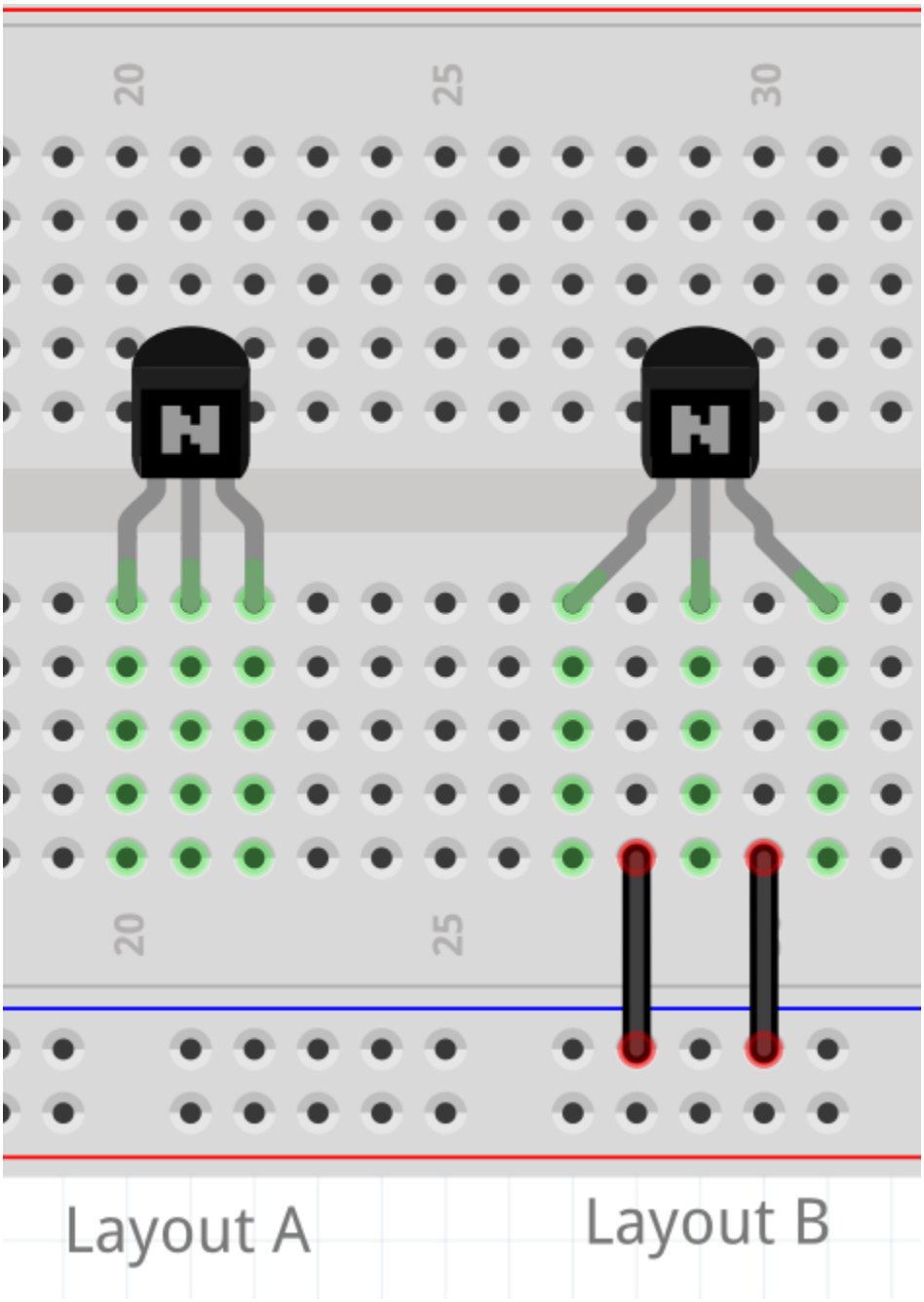

Figure 1: Different layouts for transistors.

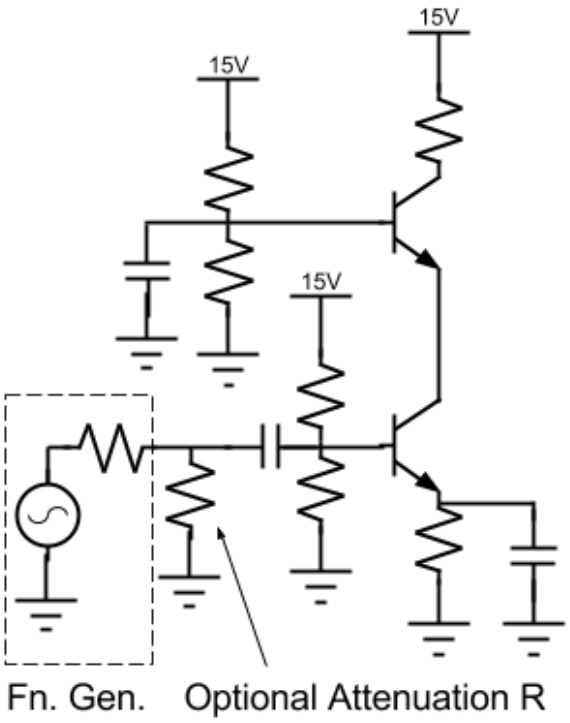

Figure 2: A sample design for a cascode amplifier.

3 Compare Cascode Amplifier Measurements to OCTC

Design a cascode amplifier using the reference design pictured in Figure 2 such that it has a gain of 120 and collector current of 1mA. Use the same R_c, R_e, C_e etc. as the common emitters in the last section. Use layout B for the NPN devices. One explicit challenge of the lab is deciding what the bias voltage of the common base stage's base should be. Another challenge is applying open circuit time constants to the circuit in order to get an accurate prediction of the bandwidth of the circuit. A third is that this design is sometimes unstable, remove the capacitor on the common base's base if you have stability issues (which you can see in transient simulations or in measurements, but not in AC or OP simulations).

You must start this lab by making hand calculations that predict the amplifier specifications and bandwidth. These hand calculations should include calculations of open circuit time constants. After that you should simulate your design to make sure those component values work in simulation. Finally, you must build your design and measure r_{in}, r_{out}, a Bode plot of a_v and a step response for your Cascode.

Plot bode plots of measured, simulated and OCTC analytical a_v on the same axis and justify any differences between them. The expectation in this lab is that you will refine your design, measurements and models until you get fairly good agreement (OCTC may be off my as much as 50% in the worst case, but you should do better than that).

Compare the corner frequencies and V_{SW} of amplifier B wtih your cascode amplifier and comment on the design tradeoffs between the two circuit topologies.

For extra credit, you may repeat the steps of this section to calculate and model your short circuit time constants and the bottom corner of the mid-band as well.

Required Data: Schematic of cascode amplifier, values for r_{in}, r_{out} and V_{SW}, the bode plot requested above, some OCTC calculations, comparison between cascode and common emitter