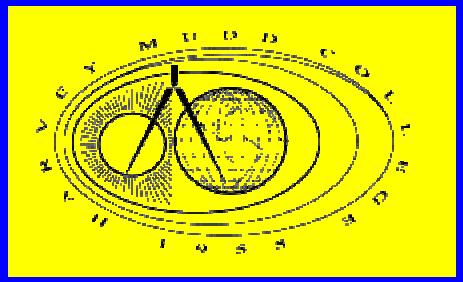
CMOS VLSI Design

David Harris
Harvey Mudd College
Claremont, CA 91711
[David_Harris@hmc.edu]



VLSI Education

- History
- Textbooks
- Present Questions
- CAD Tools
- Textbook Philosophy
- Class Examples
  - E158: Introduction to CMOS VLSI Design
  - FYS1: Digital Electronics & Chip Design

History

- Until 1978, integrated circuits were a black art
- VLSI was born with Lynn Conway's 1978 class at MIT
  - Mead & Conway, *Intro to VLSI Systems*
  - 1979-80: 12 universities teaching VLSI
  - 1982-83: 113 universities teaching VLSI

MIT VLSI Class

- Undergrads, grad students, faculty

Photos courtesy Lynn Conway
http://ai.eecs.umich.edu/~mirror/MIT78/MIT78.html

Syllabus

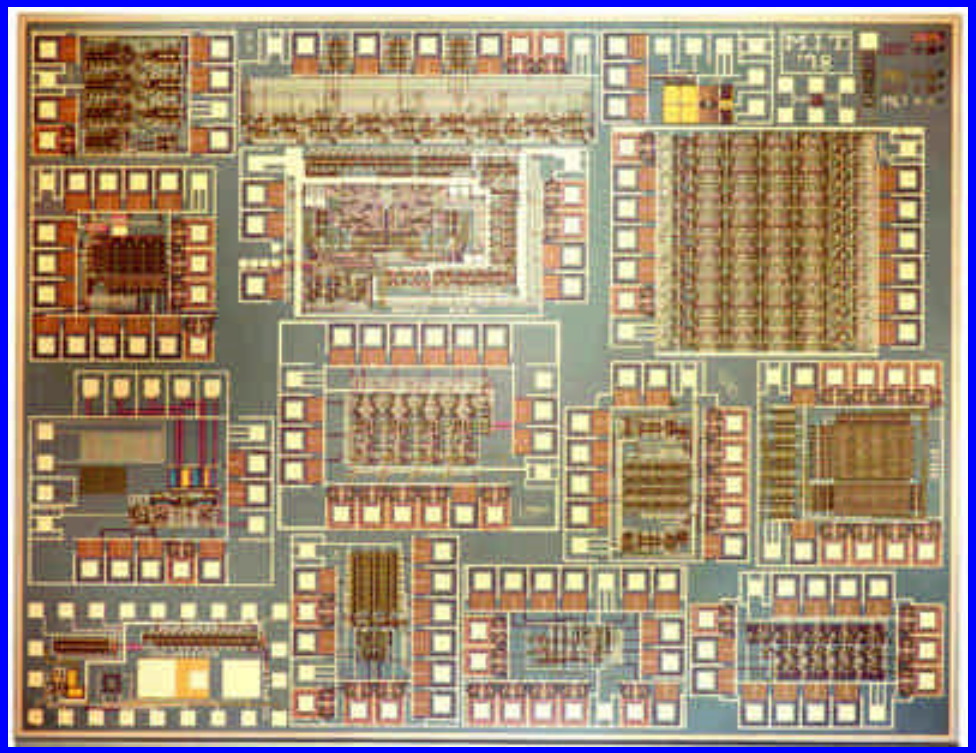
Session	Topic
00000	Overview
00001	MOS Transistors, Logic gates
00010	Timing
00011	Comb. and seq. circuits
00100	Fabrication
00101	Layout
00110	Delay optimization
00111	PLAs and datapath subystems
01000	CAD
01001	Project administration
01010	Yield and timing
01011	Design methodology
01100	Case study: Processor
01101	Case study: CAD
01110	Midterm
01111	Scaling
10000	Scaling limits
10001	Future fabrication
10010	Memory systems
10011	Case study: Speech processing
10100	Case study: Electrical characterization
10101	Project reviews
10110	Case study: Concurrent systems
10111	Case study: Recursive machines
11000	Project summaries, wrap-up

Design Flow

- Symbolic layout
- CIF output
- Sent to Xerox over ArpaNet
- Multiproject chips
- 1-month fab @ HP
- MOSIS
- Mostly operational

Projects

- **Multiproject chip set**



- D/A Converter
- PLA
- Processor bitslice
- LISP processor
- FIFO
- Cache LRU
- Bubble sort mem

http://ai.eecs.umich.edu/~mirror/MPCAdv/MPCAdv.html

VLSI Textbooks

- **1972**

  Penny & Lau, *MOS Integrated Circuits*
- **1980**

  Mead & Conway, *Introduction to VLSI Systems*
- **1985**

  Weste & Eshraghian, *Principles of CMOS VLSI Design*

  Glasser & Dobberpuhl, *Design and Analysis of VLSI Circuits*
- **1993**

  Weste & Eshraghian, *Principles of CMOS VLSI Design (2e)*
- **1996**

  Rabaey, *Digital Integrated Circuits, A Design Perspective*

VLSI Textbooks

- **1997**

  Smith, *Application-Specific Integrated Circuits*

- **2002**

  Kang & Leblebici, *CMOS Dig. Int. Ckts. Analysis and Design* (3e)

  Uyemura, *Introduction to VLSI Circuits and Systems*

  Wolf, *Modern VLSI Design* (3e)

- **2003**

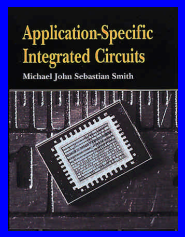
  Rabaey et al., *Digital Integrated Circuits, A Design Perspective* (2e)

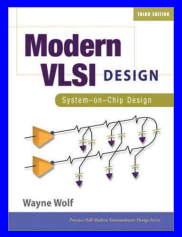
- **2004**

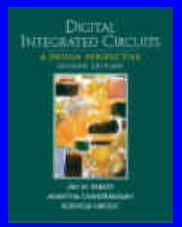
  Hodges, Jackson, & Saleh, *Analysis and Design of Dig. Int. Ckts.* (3e)

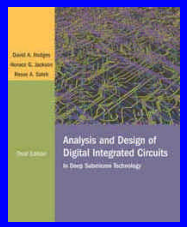
  Baker, *CMOS: Circuit Design, Layout, and Simulation* (2e)

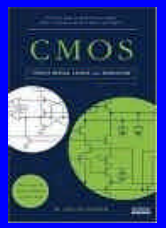
  Weste & Harris, *CMOS VLSI Design* (3e)

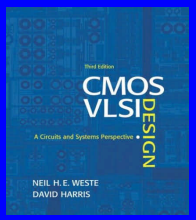












Present Questions

- What should CEs/EEs know about VLSI?
- When should VLSI be taught?
- How does the rise of synthesis affect VLSI education?
- Where does VLSI fit in the analysis vs. design continuum?
- Should VLSI courses involve custom layout?
- How do FPGAs affect VLSI education?
- How do SOCs affect VLSI education?
- How does globalization affect VLSI education?

CAD Tools

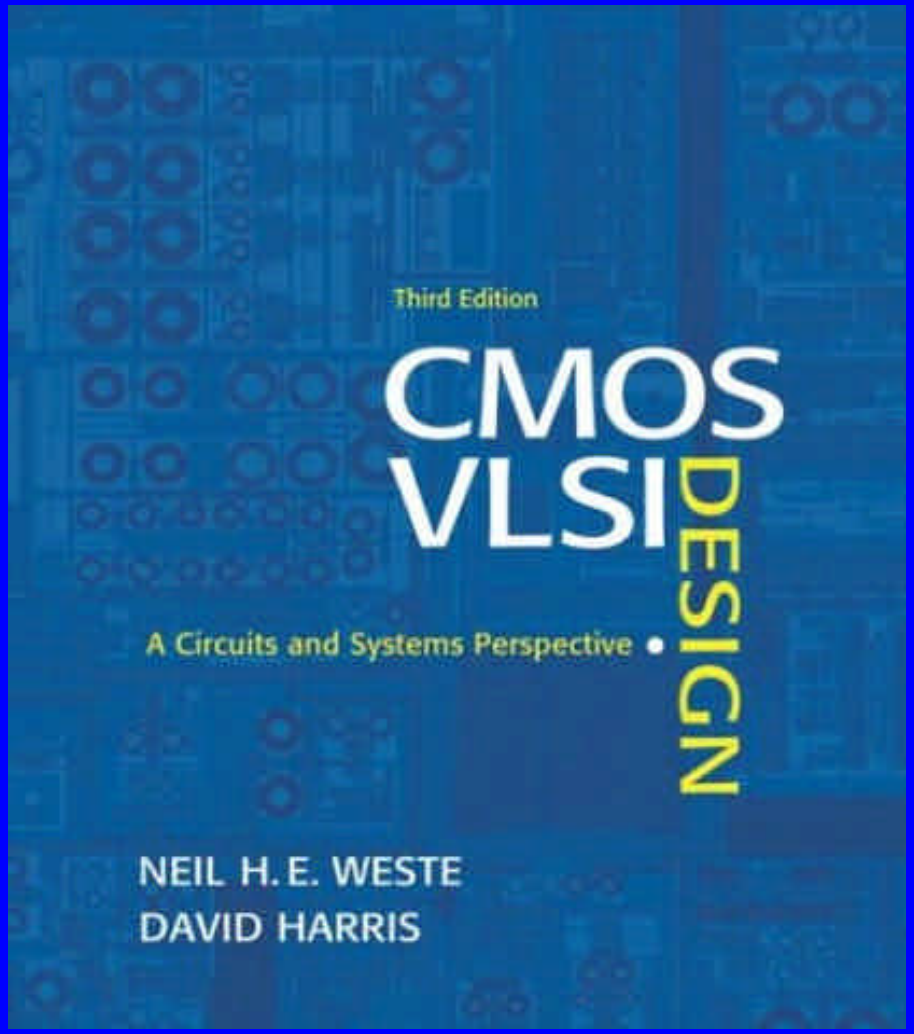
- Cadence
- Mentor
- Tanner
- Magic
- Electric

- SPICE / HSPICE
- Design Compiler

CMOS VLSI Design Book

1) Introduction
2) Devices
3) Fabrication
4) Circuits
5) SPICE
6) Comb. Circuits
7) Seq. Circuits
8) Methodology
9) Test
10) Datapaths
11) Arrays
12) Special Purpose Systems

A) Verilog
B) VHDL



Audience

- Chapter 1 jumpstarts design
  - Gives enough background to start building a chip
  - First half is accessible to freshmen
  - MIPS processor case study builds on Patterson & Hennessy
- Book suitable for intro junior/senior level course
- Advanced topics through second-level graduate courses

Philosophy

- Focus on design over analysis
  - Few equations, limited nasty physics
  - Intuitive approach appeals to students
- Real circuits
  - Emphasizes circuits used on commercial products
  - Attempts to evaluate, not just catalog
- Reference value
  - Err on side of being comprehensive rather than brief
- Teaching by example
  - SPICE, Verilog, VHDL

Instructor Supplements

- Exercise Solutions
- Lecture Slides
- Laboratory Assignments
- Electronic figures and code
- Hyperlinked References (ieeexplore)
- CAD tool links
- Way too much errata

www.cmosvlsi.com

E158: Intro to CMOS VLSI Design

- Taken by HMC juniors and seniors
  - Mostly general engineering majors
  - Occasionally CS, Math, Bio
  - 15-30 students
- 3 units spring semester
- Project-based class

www3.hmc.edu/~harris/class/e158

Guided vs. Open-Ended Projects

- "*You cannot create experience – you must undergo it*." Albert Camus
- Guided Project
  - + Focus students on key concepts
  - + Less time consuming
- Open-Ended Project
  - + Exciting for students
  - + Teaches general design skills
- In E158, we do both

Goals

Upon completion of E158, the successful student will be able to:

1. **Use the Electric CAD tool to build an 8-bit MIPS microprocessor including**
   a. **Schematic entry**
   b. **Layout**
   c. **Transistor-level cell design**
   d. **Gate-level logic design**
   e. **Hierarchical design**
   f. **Switch-level simulation (IRSIM)**
   g. **Design rule checking (DRC)**
   h. **Electrical rule checking (ERC)**
   i. **Network consistency checking (NCC)**
   j. **HDL design (Verilog)**
   k. **Logic synthesis (Synopsys Design Analyzer)**
   l. **Place and route**
   m. **Pad frame generation and routing**
   n. **Pretapeout verification**

Goals

2. Design one's own custom integrated circuit from concept through tapeout including
   a. Team design skills and partitioning
   b. Specification
   c. Logic design
   d. Circuit design
   e. Floorplanning and physical design
   f. Design verification
   g. Tapeout

Goals

3. Estimate and optimize combinational circuit delay using RC delay models and logical effort
4. Simulate circuits with HSPICE and tune for performance
5. Estimate and optimize interconnect delay and noise
6. Design for higher performance or lower area using alternative circuit families
7. Describe and avoid common CMOS circuit pitfalls and reliability problems
8. Compare the tradeoffs of sequencing elements including flip-flops, transparent latches, and pulsed latches
9. Design functional units including adders, multipliers, ROMs, SRAMs, and PLAs
10. Describe the sources and effects of clock skew
11. Predict the capabilities of future CMOS processes using scaling theory and the SIA roadmap
12. Evaluate the economics of integrated circuit design

Syllabus

00000	19-Jan	Introduction and overview	1.1-1.4	
00001	24-Jan	Circuits, fabrication, and layout	1.5	
00010	26-Jan	Microprocessor example	1.6-1.12	Lab 1 due
00011	31-Jan	CMOS transistor theory	2.1-2.3	PS 1 due
00100	2-Feb	DC and transient response	2.5-6, 4.1-4.2	Lab 2 due
00101	7-Feb	Logical effort	4.3	PS 2 due
00110	9-Feb	-- Silicon Run Video --	3.1-3.8 (skim)	Lab 3 due
	14-Feb	Interconnect engineering	4.5-4.6	PS 3 due
00111	16-Feb	Simulation	5.1-5.3	Lab 4 due
01000	21-Feb	Combinational circuit design	6.1-6.2.1	Preliminary prop due
01001	23-Feb	Circuit families	6.2.2-6.2.5	Lab 5
01010	28-Feb	Sequential circuit design	7.1-7.3.6	Project proposal due
01011	2-Mar	Adders	10.1-10.2	PS 4 due
01100	7-Mar	Datapath functional units	10.3-10.9	
01101	9-Mar	TBD		Floorplan due
	14-Mar	– Spring Break: No Class –		
	16-Mar	– Spring Break: No Class –		
01110	21-Mar	Memories	11.1-11.2	
01111	23-Mar	Memories	11.5-11.7	Schematics complete
10000	28-Mar	Non-ideal transistor characteristics	2.4	PS 5 due
10001	30-Mar	Low power guest lecture: Dr. Ram Krishnamurthy	4.4, 6.5	
10010	4-Apr	In-class design reviews		Leaf cells complete
10011	6-Apr	In-class design reviews		
10100	11-Apr	Design margining and circuit pitfalls	4.7-4.8, 6.3	
10101	13-Apr	Design for testability	9.1-9.7 (skim)	Final Project due
10110	18-Apr	Skew-tolerant circuit design	7.5.1-7.5.2	
10111	20-Apr	Packaging, I/O, & clock and power distribution	12.1-12.5	PS 6 due
11000	25-Apr	Scaling and economics	4.9, 8.5	
11001	27-Apr	A History of Intel Microprocessor Chips	4.10-4.11	

Note: Final project presentations will take place during presentation days (May 4).

Syllabus

Session`	MIT VLSI Class (1978)	HMC VLSI Class (2005)
00000	Overview	Overview
00001	MOS Transistors, Logic gates	Logic gates, layout
00010	Timing	Case study: MIPS processor
00011	Comb. and seq. circuits	CMOS transistors
00100	Fabrication	DC and transient response
00101	Layout	Logical effort
00110	Delay optimization	Fabrication
00111	PLAs and datapath subsystems	Interconnect
01000	CAD	Simulation
01001	Project administration	Combinational circuits
01010	Yield and timing	Circuit families
01011	Design methodology	Sequential circuits
01100	Case study: Processor	Adders
01101	Case study: CAD	Datapath units
01110	Midterm	SRAM
01111	Scaling	Memories
10000	Scaling limits	Nonideal transistors
10001	Future fabrication	Low power design
10010	Memory systems	Project reviews
10011	Case study: Speech processing	Pitfalls, yield and reliability
10100	Case study: Electrical characterization	Testing
10101	Project reviews	Skew-tolerant circuits
10110	Case study: Concurrent systems	I/O, Packaging, power
10111	Case study: Recursive machines	Scaling
11000	Project presentations	Case study: Intel microprocessors
11001		Project presentations

Grading

- Labs: 40%
- Final Project: 45%
- Problem Sets: 10%
- Activities: 5%

Labs

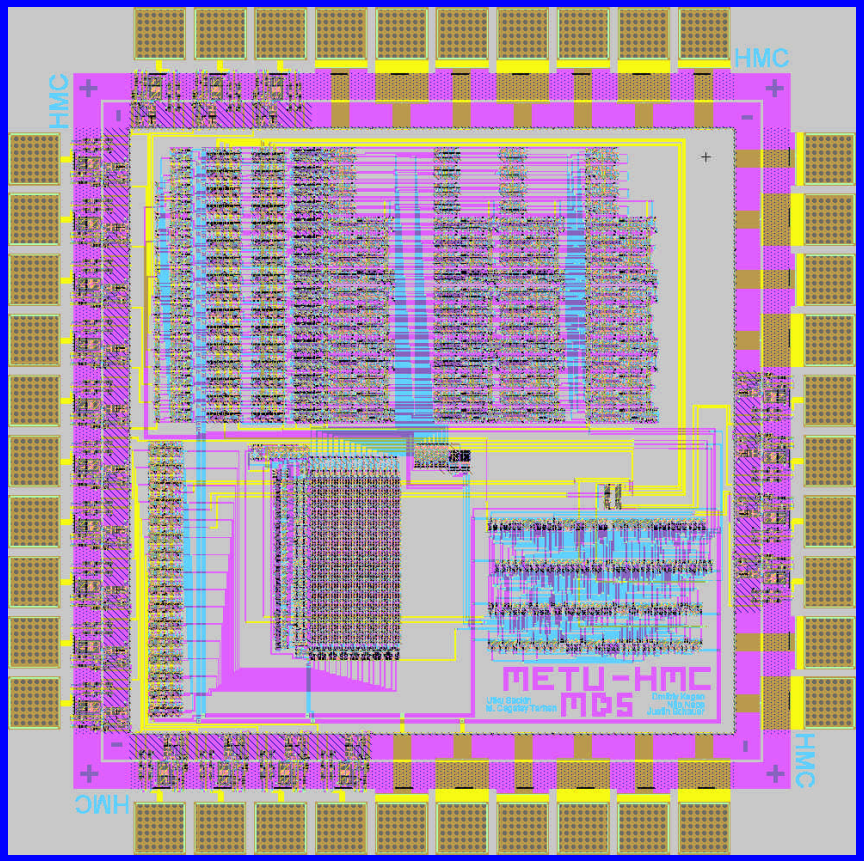
- Become familiar with Electric
- Learn design process
  1. Basic gate design
  2. Full adder design
  3. ALU, bitslice, datapath
  4. Controller Verilog & Synthesis
  5. Full-chip assembly

Project

- Team final projects
  - Groups of two
  - Choose own topic
  - Fit on 40-pin 0.5 μm MOSIS TinyChip
- Milestones
  - Proposal
  - Revised proposal
  - Floorplan
  - Schematic
  - Layout
  - Final Presentation

Project Examples

- Alarm clock
- Domino multiplier
- Lights out game
- FIR filter
- GPS searcher
- Audio DSP
- Lookahead adder
- MD5 Decryption



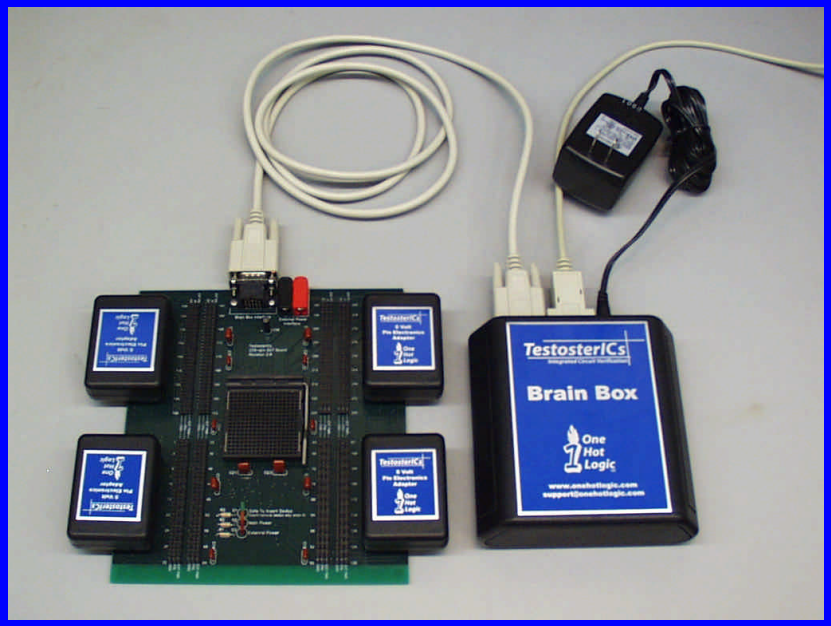
IC Fabrication

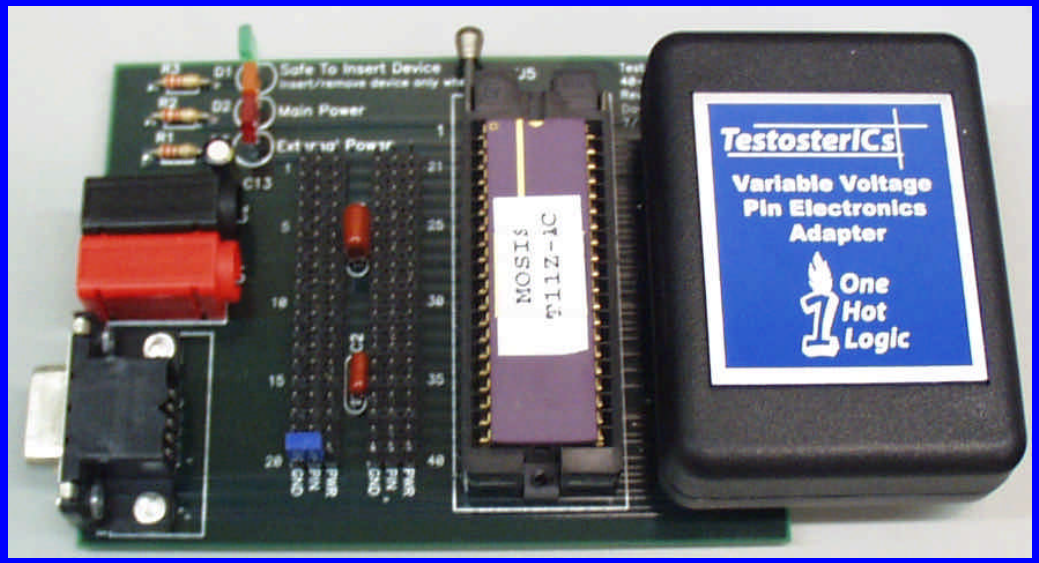
- SIA Funding for fabrication
  - 3-4 chips per year
  - Competitive selection
- Students find real chips exciting
- Chips back by August

Testing

- Students commit to testing chips after fabrication
- Requires a junior on each team that builds a chip
- Use TestosterICs chip tester
  - Inspired by MacTester (U. Washington)
- Apply IRSIM test vectors
- Good success rate

TestosterICs





www.onehotlogic.com

Testing Homework

- Not all students fabricate chips
- Test an existing chip on homework
  - Inspired by Tina Hudson (Rose-Hulman)
  - Chip designed by freshmen
  - Test circuits, some with intentional errors
    - Missing contact in layout
    - Bad P/N ratio in pseudo-nMOS inverter
  - Produce test vectors, diagnose failures

Workload

- VLSI classes are notorious time sinks
- Average workloads:

Lab	Hours
1	6.4
2	9.9
3	12
4	8.5
5	7.5

Problem Set	Hours
1	4.2
2	2
3	3.3
4	6.3
5	5
6	2

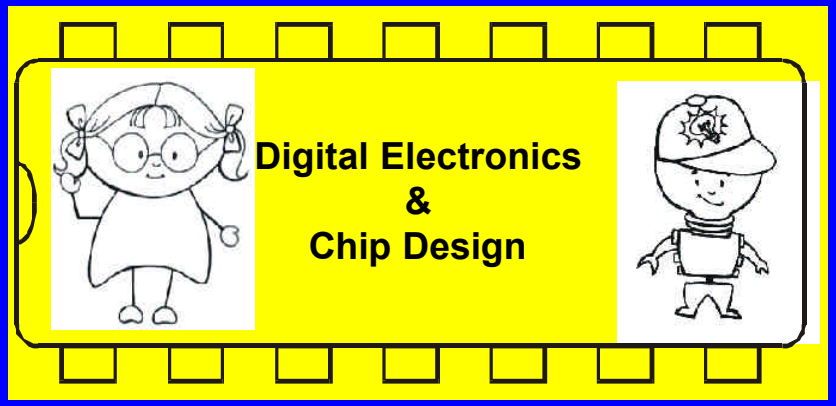
  - Final project: 50 – 200 hours / team
- Total average: 12 hours/week
  - Frontloaded to avoid conflicts

Assessment

- Students enjoy subject material
  - Typical course evaluations: 6.5/7
  - Pride in designing own chip
  - Many get jobs in VLSI
- Inexpensive
  - Modest fees for Synopsys & HSPICE
    - Used for research as well
  - Electric is free
  - Fabrication supported by SIA

FYS1: Digital Electronics & Chip Design

- Freshman advising seminar



- What do engineers really do?
- Frosh explore major before choosing
- I get to know advisees, groom research students

Course Organizatoin

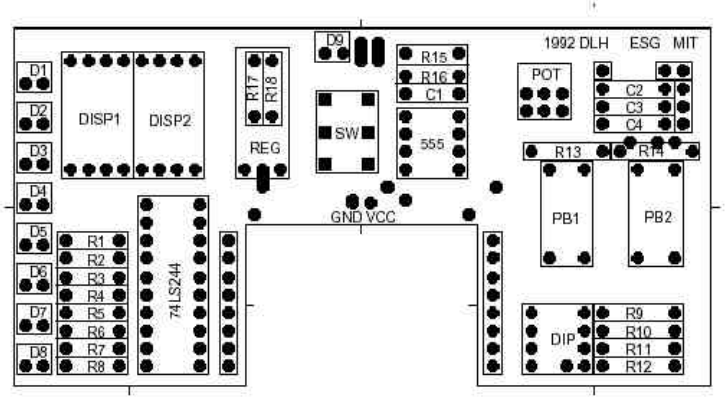
- Participants:
  - Advisor, 6-8 freshmen, lab assistant
- Schedule
  - Fall 1999-2004
  - 13 seminar meetings (Wednesday 18:30-22:30)
  - One hour lecture, 2-3 hours of supervised lab
  - Usually one optional Saturday tapeout party
- Credit
  - 1 unit pass/fail credit (based on attendance)
  - Lab assistants get campus wages or credit

Syllabus

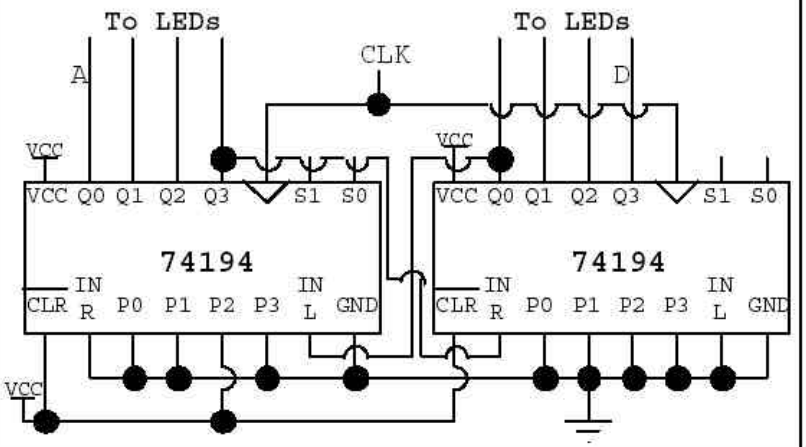
Date	Topic	Lab
8/25	*Orientation Beach Trip*	
9/5	Lights, switches, & soldering	Assemble utility board
9/12	Logic gates	Breadboard simple combinational digital circuit
9/19	Boolean algebra	Design and breadboard combinational digital circuit
9/26	Sequential circuits	Flip-flop experiments
10/3	Finite state machines	Pocket hypnotizer
10/10	CMOS circuits	Schematic entry of inv, nand, nor, and, or, tristate, latch
10/17	CMOS layout	Layout of inv, nand, nor, and, or, tristate, latch
10/24	*Fall break: no seminar*	
10/31	Structured layout	Complete schematics and layouts
11/7, 14, 21	Project	Team implementation of project
11/28	*Thanksgiving: no seminar*	
12/5	Project	Continue project
12/12	End of class party	Tapeout

Labs

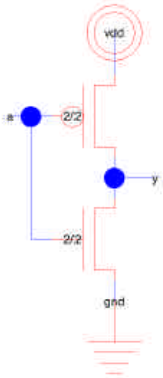
Utility Board



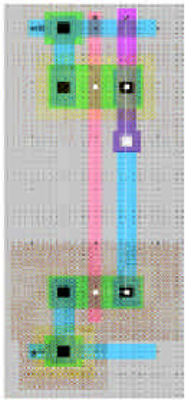
Pocket Hypnotizer



Electric Schematic Editor

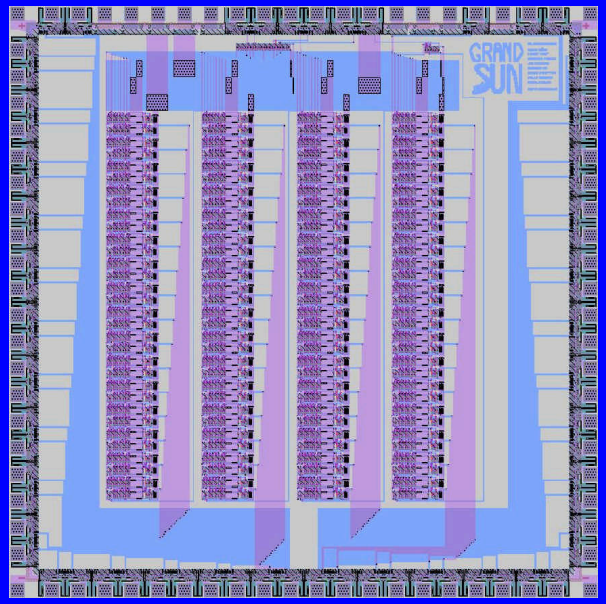


Electric Layout Editor



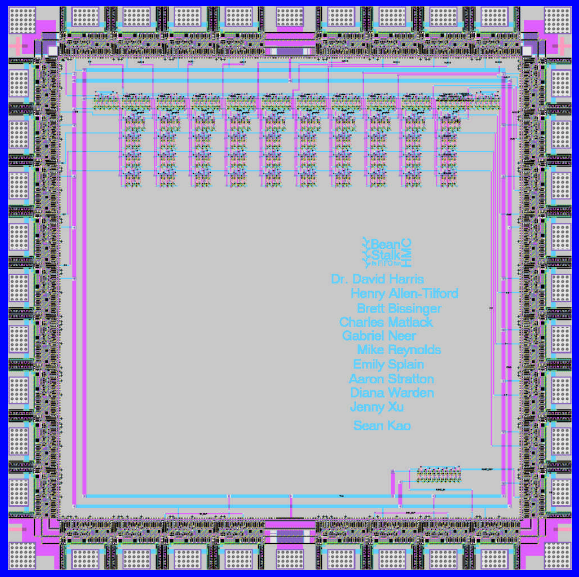
1999: *GrandSun of MacTester*

- Supporting Sun Microsystems Clinic
- Chip tester pin electronics chip
- Spun off start-up with student, David Diaz, to commercialize chip testers



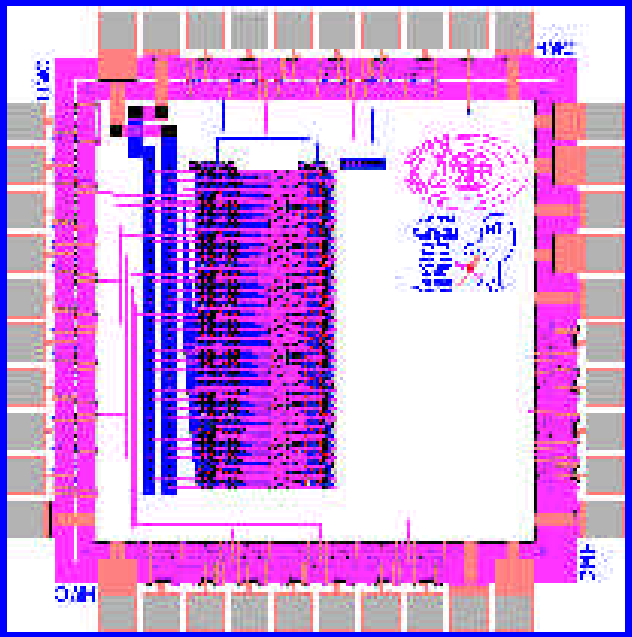
2000: PhiFIFOFun

- Supporting Sun Microsystems Clinic
- Asynchronous FIFO chip
- Verification problems with new Electric
- Partially operational



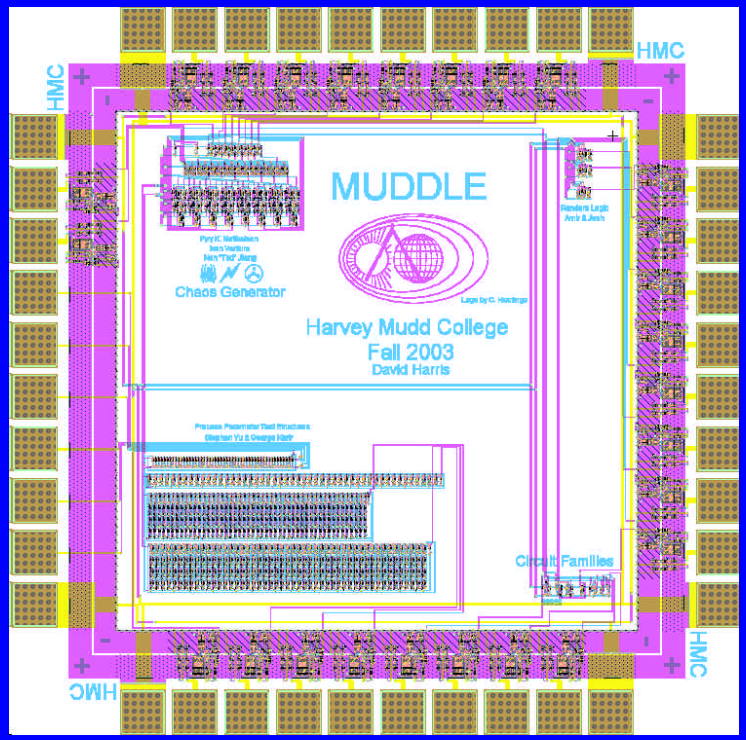
2001: *QBERT*

- Supporting Aerospace Corp. Clinic
  - Quick Bit Error Rate Tester
  - Fully operational low-speed proof of concept



2003: Muddle

- Test structures for E158 testing HW
- Freely available on E158 site



Assessment

- ~70 freshmen per year apply
- Teaching evaluations: 6.2-6.8 / 7
- Freshmen are remarkably capable
  - Valuable chips
  - Six seminar grads have become research students
  - Three have cotaught the seminar
- Intangible advising benefits

Costs

- $50/student for PCB, supplies
- $40/student orientation activity
- $450/semester lab assistant
- 5 hours/week faculty time
  - 10 hours prep before semester
  - Much more the first time
  - Mostly uncompensated
- Chip fabrication through SIA

Graduate Courses

- Digital Integrated Circuits
  - Devices, circuit analysis
- Advanced VLSI
  - Design for speed and low power
  - SPICE
- System-on-chip
  - IP reuse, high level modeling

Summary

- VLSI fundamentals scarcely changed
  - Exposes “black magic” to students
  - Make layers of abstraction concrete
  - Understand physical design impact on circuits and logic
  - Major design project experience
- Subject is accessible to freshmen

Revisit Questions

- What should CEs/EEs know about VLSI?
- When should VLSI be taught?
- How does the rise of synthesis affect VLSI education?
- Where does VLSI fit in the analysis vs. design continuum?
- Should VLSI courses involve custom layout?
- How do FPGAs affect VLSI education?
- How do SOCs affect VLSI education?
- How does globalization affect VLSI education?