Bias Dependence of Single-Event Upsets in 16 nm FinFET D-Flip-Flops

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***Abstract*—With fabrication processes migrating from planar devices to FinFETs, the differences in physical structure necessitate evaluating the SEU mechanisms of FinFET-based circuits. Since FinFET-based bi-stable circuits have shown better stability at low supply voltages and hence improved power dissipation, it is also necessary to assess the SEU performance over a range of voltages. In this work, the SEU cross section of FinFET-based D-flip-flops was measured with alpha particles, protons, neutrons, and heavy-ions. Results show a strong exponential increase in the SEU rate with reduction in bias for low-LET particles. Technology Computer Aided Design (TCAD) simulations show that the weak variation of collected charge with supply voltage, combined with the standard bias dependence of critical charge, is responsible for this trend.**

***Index Terms*—Single Event, Soft Error, FinFET, SER, Alpha particles, Neutrons, Heavy-ions, Protons, Latch, Flip-Flop.**

I. Introduction

A major design challenge for the electronics industry is the overall power dissipation of integrated circuits (ICs). The Semiconductor Industry Association (SIA) roadmap has identified power dissipation as one of the key reliability concerns for future electronic systems [1]. Since power dissipation is proportional to V_{DD}^2, system-level designers have resorted to reducing the supply voltage to reduce power. With technology scaling and the aforementioned reduction in the supply voltage, single-event upset (SEU) vulnerability of storage cells has emerged as another major reliability concern [2, 3]. Although mitigating SEU effects for arrayed memory cells with error-correcting codes (ECC) or other error detection/correction schemes is easy, protecting flip-flops against SEUs is difficult or requires the use of design-hardening solutions that have performance tradeoffs. With increasing packing densities, the increasing number of flip-flop (FF) cells on an IC results in IC-level SEU error rates dominated by upsets in unhardened FF designs. In addition, the technology scaling from planar to FinFET or tri-gate processes calls for a detailed understanding of the SEU response of FinFET-based circuits. El-Mamouni et al. showed that the sensitive area for charge collection in bulk FinFETs is larger than the fin structure, indicating a possible increase in SEU cross sections [4]. The devices used in [4] were characterized by large drain areas, which seem to explain the trend observed. However, experimental and simulation results reported on a range of FinFET processes used in large scale manufacturing indicate a reduction in the sensitive cross-section area of individual transistors, resulting in better per-bit SEU performance, especially for nominal supply voltage operation [5 – 7]. For example, Seifert et al. reported more than three times reduction in per-bit SEU error rates for FinFET designs for terrestrial environments dominated by neutrons and alpha particles compared to a similar sized, planar process at a nominal operating voltage [5]. Similar scaling trends in the per-bit SEU error rates were observed in this work for standard D-flip-flop designs operating at nominal voltage as shown in Fig. 1.

The above mentioned works on FinFET SEUs have generally focused on the response at close to nominal supply voltages, but little is known about the SEU sensitivities for reduced supply voltages. Compared to planar technologies,

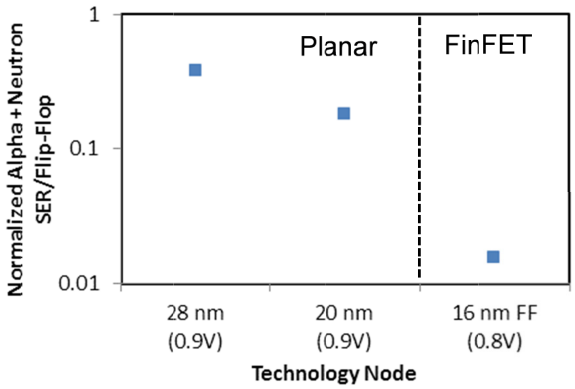

Fig. 1. Normalized per-bit alpha + neutron SE error rate scaling trend for standard D-flip-flop design operating at nominal voltage.

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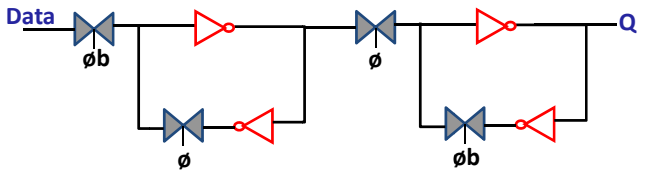

Fig. 2. Schematic of a standard transmission gate-based D-flip-flop.

FinFET technology has better stability and current drive at reduced supply voltages because the gate controls the channel from three-sides [8, 9]. This allows designers to reduce the supply voltage to achieve the desired reduction in power dissipation. Since designers are proposing to use reduced-supply voltages for FinFET technology, it has become imperative to evaluate the low-voltage SEU sensitivity of FinFET-based FF designs.

Prior simulation-based works on SOI and bulk FinFET processes have shown a strong bias dependence for SRAM and combinational logic SEU [10, 11]. Experimentally-determined flip-flop SEU trends across a wide range of bias and particle types in a FinFET process have not been reported previously. Furthermore, most previous experimental data on planar technologies show a weak exponential dependence or strong linear dependence for SRAM and flip-flops on supply voltage [12 – 14]. In [13] a wide range of flip-flops fabricated in a 40 nm technology were shown to have a linear dependence of SEU rate on supply voltage. In [14], the dependence was shown to vary, depending on the flip-flop design. For standard DFF designs that follow standard layout rules, the reported trend is described by a weak exponential, while a stronger bias dependence was reported for a design using modified layout rules. In general, the SEU increase from nominal bias to very low bias (near the lowest stable operating voltage) is less than an order of magnitude for DFF designs that follow standard layout practices in planar process, while the data presented in this work shows an increase of more than two orders of magnitude in alpha SEU for the finFET process, over a comparable voltage range. Since the operating voltage range of FinFET processes is generally larger than that of planar processes, the issue of bias dependence for FinFETs is more important than that of planar processes. The results highlight that FinFET processes may not offer the same SEU benefits over planar processes at low bias that they do at nominal bias.

In this work, SEU cross sections were measured as a function of supply voltage for 16 nm FinFET D-flip-flops with low-energy protons, alpha particles, high-energy neutrons, and heavy-ions. The results show a strong exponential increase in SEU cross section with decreasing bias for low-energy protons and alpha particles, while the increase is less pronounced with high-energy neutrons. Data for the same type of flip-flop design fabricated in planar 28-nm and 20-nm processes show linear (or weak exponential) trends with bias. This is the first study on flip-flop designs fabricated in a bulk FinFET process showing a strong exponential dependence of SEU cross section on supply voltage for low LET particles. The trends are important not only for space applications, but also for most terrestrial applications. Heavy-ion test results indicate strong exponential dependence of the SEU cross sections with bias for low-LET particles while the trend is mildly exponential or linear-like with high-LET particles. 3D-TCAD simulation results show that the physical FinFET structure, as well as carrier diffusion processes, are responsible for this behavior. These results highlight the importance of understanding SEU mechanisms for FinFET-based circuits as well as developing mitigation schemes based on the intended operating voltage range and environment for FinFET-based designs.

The rest of the paper is organized as follows. In section II, the test chip design is described. Section III provides the alpha particle test results for planar and FinFET flip-flop designs, along with a discussion of the physical mechanisms using TCAD simulations. This discussion not only helps in understanding the alpha-particle trends, but also in predicting

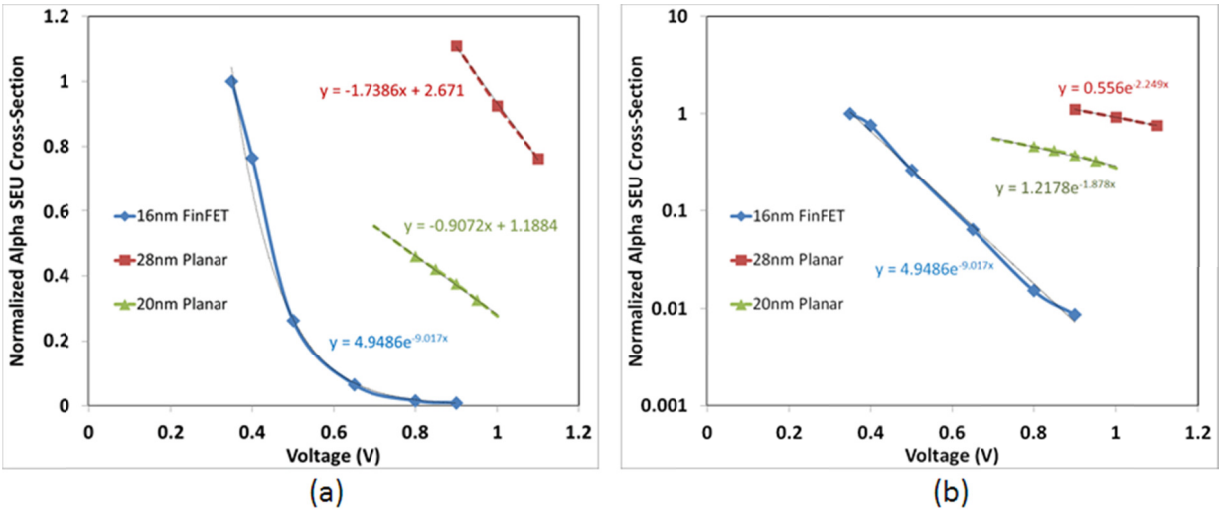

Fig. 3. (a) Normalized alpha-particle induced SEU cross-section (using linear y-axis scale) versus voltage for 16 nm FinFET, 28 nm planar, and 20 nm planar processes. (b) Same chart using log-y-axis illustrates how the planar processes SEU trends fit both a linear and well as an exponential trend with a small exponent.

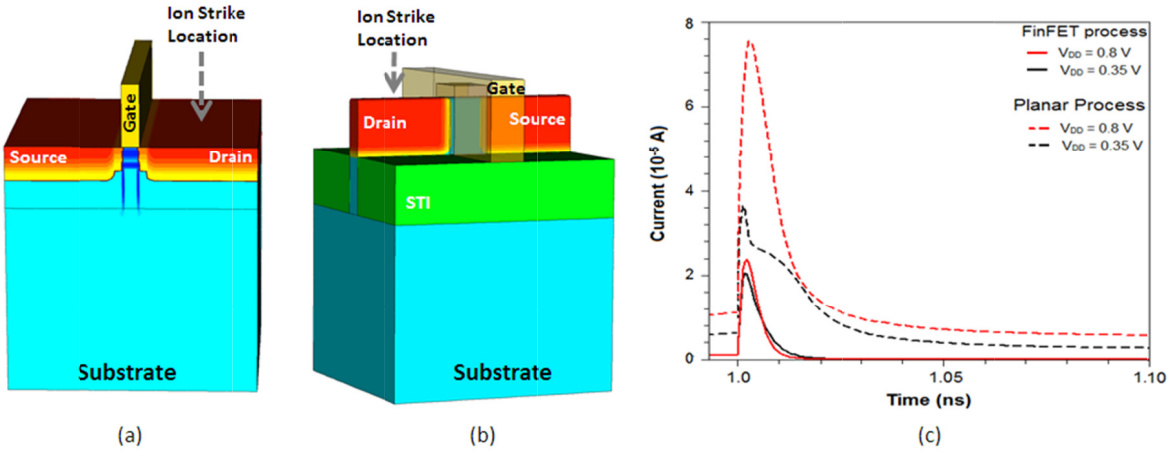

Fig. 4. 3D-TCAD model of (a) planar and (b) FinFET n-channel transistor showing the ion-strike location. (c) Mixed-mode TCAD simulation results for LET = 1 MeV-cm^2/mg showing the current pulse waveforms for the 20 nm planar and 16 nm FinFET processes.

the behavior of the FinFET design for other particle types. Section IV presents test results for proton, neutron, and heavy-ion irradiations that agree with the mechanisms discussed in Section III. Section V concludes the paper.

II. Test Chip Design

A test chip containing 48K standard D-flip-flops was designed and fabricated in a commercial 16 nm FinFET process. Fig. 2 shows the schematic of a standard transmission-gate based edge-triggered D-flip-flop. It is composed of two latches, each designed with back-to-back connected inverters. The flip-flops were implemented in the form of a register array. Tests were conducted in static mode with solid test patterns to minimize the influence of clock upsets. One nominal power supply voltage option for this process is 0.8 V. Devices were tested to demonstrate stable operation at supply voltages as low as 0.3 V.

III. Alpha Particle-Induced Single-Event Upsets

A. Experimental Results

Alpha-particle tests were conducted using an Americium-241 5.5 MeV alpha source with an activity of about 10 µCi. Data was collected for All-0 and All-1 patterns. The all-0/1 patterns eliminate all errors due to ion hits on the clock cells. Data was collected for supply voltages ranging from 0.35 V to 0.9 V with the 16 nm FinFET test vehicle. Alpha SEU cross sections measured on similar D-flip-flop designs implemented in 28 nm and 20 nm planar processes were used for comparison.

Fig. 3(a) shows the normalized alpha-particle SEU cross section in linear scale as a function of supply voltage for the 16 nm FinFET process, along with data for the 28 nm and 20 nm planar processes. While the FinFET data increase dramatically at low supply voltages (approximately exponentially), the data for the planar processes increase more slowly (approximately linearly). Due to limitations with the test setup, the planar-process designs were not tested at very low supply voltages as with the 16 nm FinFET design. However, the data shows clear trends in the SEU cross section for all three nodes as a function of the supply voltage. Fig. 3(b) plots the same data using a log-scale for the y-axis, which illustrates that the planar data fit can be described by either a linear trend or an exponential trend with a small exponent. The FinFET process shows a strong exponential increase in cross section with reduction in bias (large exponent) compared to the planar processes which show a weak exponential or strong linear trend. The value of the exponent for the FinFET process is greater than four times the value of the exponent for the planar processes. Though the tested voltage ranges are different for the FinFET and planar process designs, it should be noted that the slope of the exponential fit (or the value of the exponent) is similar even when considering a smaller voltage range (~0.7 V to 0.9 V) for the FinFET design (comparable to the voltage range of the planar process) as is evident from Fig. 3(b). These results indicate that for FinFET technologies, SEU assessment and mitigation approaches must take into consideration the lowest operating bias for the given application and the operating environment.

B. Physical Mechanisms

The rapid increase of SEU cross sections with the reduction in supply voltage, especially with alpha particles, has not been reported previously for bulk FinFET technologies. To understand the differences, mixed-mode 3D-TCAD simulations using a minimum sized inverter design were used to study the charge collection behavior for both the 20 nm planar and 16 nm FinFET processes at nominal and reduced supply voltages. Simulations were performed using the Synopsys tools. The TCAD models were developed using information from the SIA roadmap, the Predictive Technology Model (PTM) from Arizona State University and reference [15]. The primary goal of the TCAD simulations is to obtain a qualitative understanding of the difference in charge collection behavior for planar versus FinFET transistors and hence the model was not required to be an exact match to the foundry process (which was unavailable for calibration due to proprietary concerns). One n-channel transistor in each process was modeled in 3D-TCAD as shown in Fig. 4(a) and 4(b), while compact models were used for the restoring p-

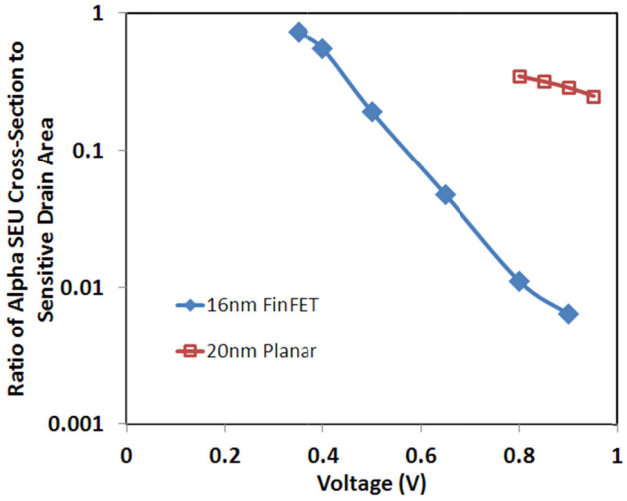

Fig. 5. Ratio comparison of the measured alpha cross-section per bit to the sensitive drain area per bit for 16 nm FinFET and 20 nm planar processes.

channel transistors. Simulations were carried out with an ion strike in the center of the drain region as this generally results in the maximum amount of charge collected by the device. Fig. 4(c) shows the current pulse waveforms at the inverter output node due to an ion strike with a linear energy transfer (LET) of 1 MeV-cm^2/mg. Simulations were run at 0.8 V and 0.35 V. The results indicate that the peak and shape of the current pulse waveform change very little in the FinFET process when supply voltage is reduced from 0.8 V to 0.35 V for these low LET particles striking the drain. The charge collected by the FinFET transistor only marginally decreases (by <3%) from 0.8 V to 0.35 V. For comparison, the planar transistor shows a decrease of more than 2× under the same conditions. The peak of the current pulse is determined by carrier drift, while the tail current is modulated by carrier diffusion. The charge collected by drift is a strong function of the depletion layer characteristics, which are strong functions of the supply voltage. On the other hand, diffusion processes are determined by the charge gradient and are generally independent of the supply voltage. This is clearly seen in Fig. 4(c) where the tail current is similar for both supply voltage values in the planar and FinFET processes. Since the sensitive drain regions are narrow fins in the FinFET structure, the collected charges are less influenced by the electric fields around the drain-body junction, resulting in similar peak currents for low-LET particles for the range of supply voltages used in this study. It should be noted that prior work by El-Mamouni et al. showed that the current pulse amplitude increases with increasing drain voltage for an SOI FinFET process [16]. However, those data were taken at higher energies (or larger charge deposition) and the devices had much larger drain areas, which potentially increase the electric-field influence on the collected charge.

The critical charge needed to upset the basic D-FF in either the 20 nm planar or the 16 nm FinFET process is comparable, since it is dominated by the node capacitance and supply voltage, and is of the order of the charge deposited by an alpha particle. For such low-LET particles, TCAD simulations show that particle hits outside of the drain region do not result in significant charge collection. As a result, alpha particles must hit the sensitive drain region directly to cause an upset for both processes. The ratio of experimentally measured alpha-particle SEU cross sections per flip-flop to the total sensitive drain area per flip-flop is shown in Fig. 5 for the 16 nm FinFET and the 20 nm planar processes. This plot shows that, at a nominal voltage (0.8 V), the SEU sensitive area is <1% of the total sensitive drain areas for the FinFET designs. For the planar process, however, the SEU sensitive drain area is >25% of the total sensitive drain areas. Since the volume of the drain is much smaller in the FinFET process, alpha particles need to traverse very close to the center of the drain or impinge at certain angles to maximize the charge collected by the drain region and hence, cause a cell upset. However, as the voltage is reduced, the amount of charge needed to cause an upset decreases (i.e., Q_{crit} decreases) and thus, effectively increases the sensitive area per transistor. For planar transistors, the effective increase in area was not significant for the range of supply voltages tested.

The reason for the strong bias dependence of FinFET SEU is explained by the well-established SEU rate model. The SEU rate has been shown to be related to the critical charge (Q_{crit}) and collected charge (Q_{coll}) by [17, 18]:

$$\textbf{SEU Rate} \propto \mathbf{e}^{-Q_{crit}/Q_{coll}} \qquad (1)$$

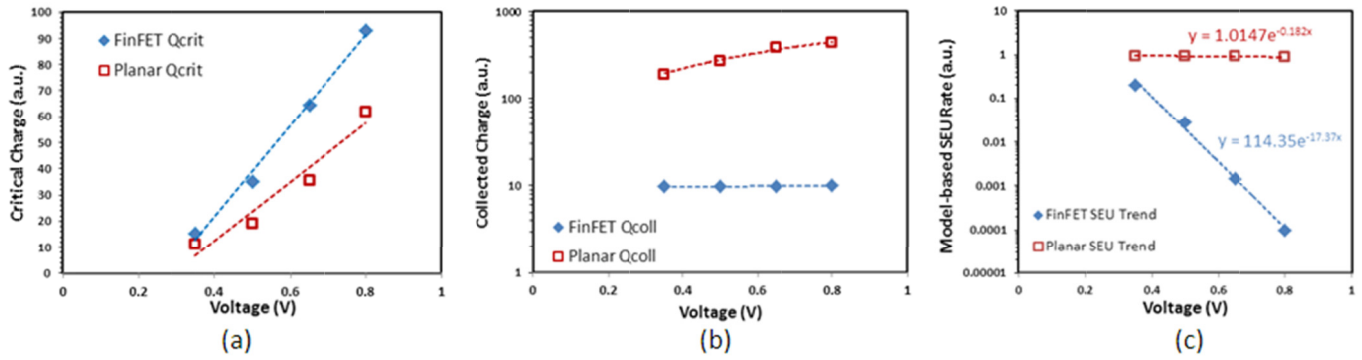

Fig. 6 (a). Critical charge trends as a function of supply voltage for 20 nm planar and 16 nm FinFET processes based on SPICE simulation, (b) TCAD simulated collected charge for planar and FinFET devices as a function of supply voltage for ion strike with LET of 1 MeV-cm^2/mg, and (c) Analytical model-based illustration of SEU trends versus bias for LET = 1 MeV-cm^2/mg.

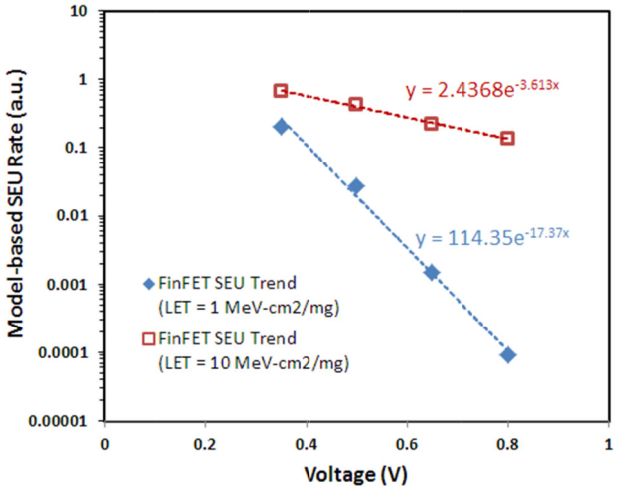

Fig. 7. Analytical model-based illustration of FinFET SEU trends versus bias based on TCAD simulated FinFET *Qcoll* for LET = 1 MeV-cm^2/mg and LET = 10 MeV-cm^2/mg.

That is, the SEU rate depends exponentially on the ratio of Q_{crit} to Q_{coll}. Fig. 6 shows an illustration of how the SEU rate would vary for the FinFET and planar processes based on this model with the TCAD-simulated Q_{coll} values for LET of 1 MeV-cm^2/mg. The Q_{crit} values are based on SPICE simulations and, as shown in Fig. 6(a), are comparable for the two processes. Circuit-level effects cause Q_{crit} to decrease with decreasing voltage in the same manner for planar and FinFET processes, as it is dominated by node capacitance and voltage. In the case of the FinFET process, Q_{coll} is smaller than that of the planar process, but relatively constant over the voltage as shown in Fig. 6(b). This difference in Q_{crit} and Q_{coll} trends results in a strong exponential dependence of SEU on the supply voltage for FinFET process (Fig. 6(c)). On the other hand, when Q_{coll} is significantly higher than Q_{crit} and both vary with voltage as in the case of the planar process, the SEU rate dependence on voltage is less pronounced and follows a more linear trend (weak exponent) as illustrated in Fig. 6(c). As described above, the TCAD model provides a qualitative comparison of the responses of circuits fabricated in FinFET and planar processes. While the modeled-SEU trend is comparable to the experimental SEU trend (strong exponential dependence predicted for FinFETs with low LET particles), the magnitude of the SEU increase (or exponent of the curve fit) predicted by the model is larger than the experimental data. In addition to the difference arising from the use of a generic model, it should be noted that the simulation was carried out for a single LET value and normal incidence, while the alpha particle charge deposition varies widely based on the particle energy and angle of incidence. The key goal of the simulation, however, is to identify the potential reasons behind the difference in the FinFET and planar SEU trends for a given particle LET.

The discussion above suggests that the increase in SEU rate at low biases is exacerbated when the charge collected due to an ion strike is comparable to the critical charge of the cell. For particles that deposit a charge similar to, or slightly lower than, that deposited by an alpha particle, similar trends will be observed. On the other hand, with particles that deposit much more charge than an alpha particle, the trend should be suppressed. Fig. 7 illustrates the model-based SEU trends for FinFET process using TCAD simulated Q_{coll} for LET of 1 MeV-cm^2/mg and 10 MeV-cm^2/mg. It shows that as Q_{coll} increases the SEU bias dependence reduces. Additional experiments with low-energy protons, high-energy neutrons, and heavy-ions with a range of particle LETs were carried out to test these claims as described in the next section.

IV. Low-Energy Proton, High-Energy Neutron and Heavy-Ion-Induced Single-Event Upsets

Low-energy proton experiments were performed at the Pelletron facility at Vanderbilt University. Since the charge deposited by low energy protons is comparable to or less than that deposited by alpha particles, similar bias dependence can be expected. Experiments were performed under vacuum conditions with a mono-energetic proton beam. Data was collected with a fixed bias for different proton energies. Low-

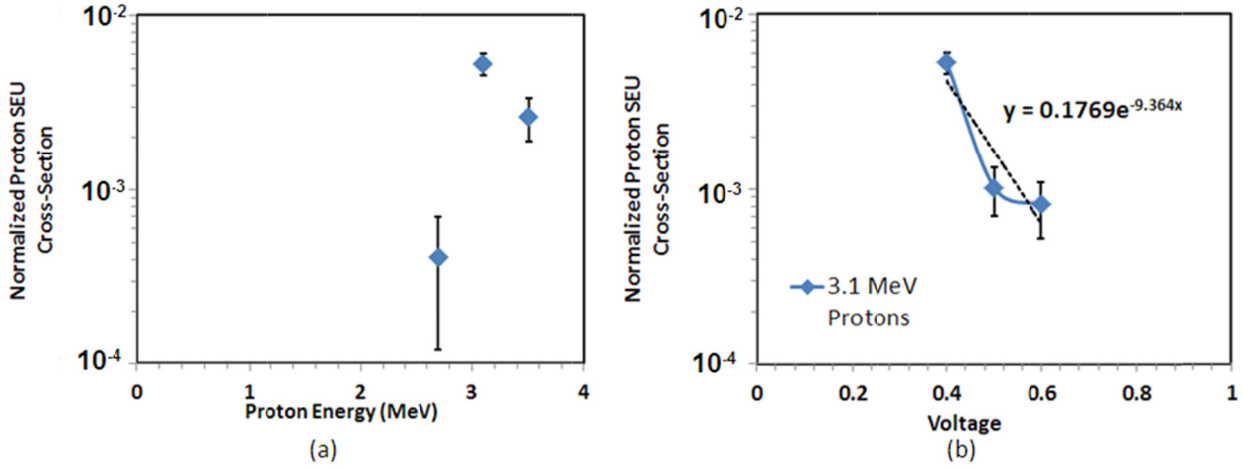

Fig. 8 (a). Normalized 16 nm FinFET D-FF proton cross-section versus proton energy showing the peak in the cross-section occurs at ~3.1MeV proton energy and (b) normalized 16 nm FinFET D-FF proton cross-section versus supply voltage for 3.1MeV protons.

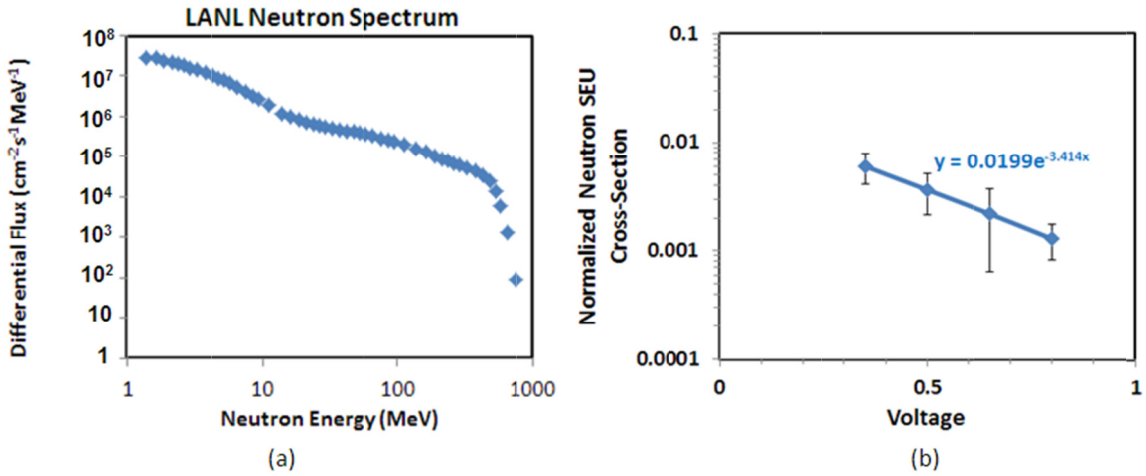

Fig. 9 (a). LANL differential neutron flux versus neutron energy which resembles the terrestrial neutron spectrum and (b) Normalized 16 nm FinFET D-FF high-energy neutron cross-section versus voltage.

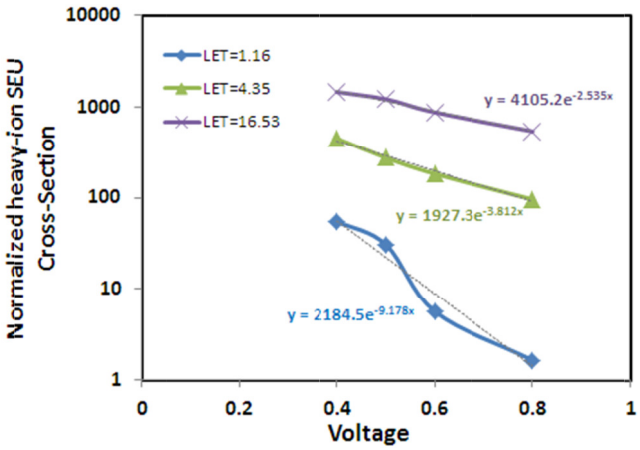

Fig. 10. Normalized 16 nm FinFET D-FF heavy-ion cross-section versus voltage. Error bars are smaller than the symbol size.

energy protons deposit charge through direct ionization, similar to alpha particles, with the cross section peaking at a certain proton energy that corresponds to maximum energy deposition in the sensitive volume as discussed in [19]. Fig. 8(a) shows the normalized proton cross section versus proton energy, showing that the peak cross section occurs with proton energy of approximately 3.1 MeV. The 3.1 MeV protons were then used for data collection at three different supply bias points. As expected, the SEU cross section increases dramatically as the supply voltage decreases, similar to the alpha SEU cross section results, as shown in Fig. 8(b).

High-energy neutron data was collected at the LANL facility with a neutron beam that resembles the terrestrial neutron spectrum with energies ranging from 1 MeV to 800 MeV as shown in Fig. 9(a). Fig. 9(b) shows the normalized neutron SEU cross section as a function of supply voltage. Neutrons generate charges through indirect ionization unlike alpha particles or low-energy protons. However, the LET range of the secondary ionizing particles from the neutron spallation reaction is generally much higher than the particle LET used in alpha and proton experiments. Thus the bias dependence of the SEU cross section for the neutron irradiations is expected to be lower compared to the alpha-particle or proton irradiations. As is evident from Fig. 9(b), the cross section trend with supply voltage for neutrons also follows an approximately exponential trend, but at a lower rate (or smaller exponent) when compared to alpha particles and low-energy protons. For instance, the ratio of the neutron cross section at 0.35 V to 0.8 V is 4.6×, while the same for alpha particles is 65×.

Heavy-ion experiments were carried out at Lawrence Berkeley National Lab (LBNL) with three different ions with linear energy transfer ranging from ~1 MeV-cm^2/mg to ~16 MeV-cm^2/mg. Data was collected for solid test patterns and over a range of voltages. All data was collected for normal incidence. Fig. 10 summarizes these test results. As expected, the lowest LET particles resulted in a strong bias dependence in the SEU cross section with a large exponent that is comparable to the alpha particle and proton data. With an increase in particle LET, and thus an increase in Q_{coll}, the SEU cross section follows a more linear trend with bias or fits an exponential with a lower exponent. The value of the exponent and hence the extent of the bias dependence of SEU cross section for the FinFET process decreases with increasing particle LET. These results again demonstrate the importance of assessing FinFET SEU as a function of bias for the intended operating environment.

V. Conclusions

With fabrication processes migrating from planar processes to FinFET or tri-gate processes, the differences in physical structures necessitate evaluating SEU mechanisms of FinFET processes. FinFET circuits are capable of stable operation at very low supply voltages, so designers of certain applications reduce the supply voltage to address power dissipation problems. This work evaluated SEU cross sections over an extensive supply voltage range for D-flip-flops designed in a FinFET process for irradiation with alpha particles, low-energy protons, neutrons, and heavy-ions. The FinFET SEU

cross section increases dramatically with a reduction in bias for low LET particles, such as alpha particles and low-energy protons. TCAD simulation results show that independence of collected charge on supply voltage is mainly responsible for the exponential increase in the SE cross section. These results indicate that SEU rates and mitigation choices for FinFET-based circuits will be strongly influenced by the supply voltage and the operating environment.

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