Surfliner: A Distortionless Electrical Signaling Scheme for Speed of Light On-Chip Communications

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Abstract

We present a novel scheme to implement distortionless transmission lines for on-chip electrical signaling. By introducing intentional leakage conductance between the wires of a differential pair, the distortionless transmission line eliminates dispersion caused by the resistive nature of on-chip wires and achieves speed of light transmission. We show that it is feasible to construct distortionless transmission line with conventional silicon process. Simulation results show that using 65nm technology, the proposed scheme can achieve 15Gbits/s bandwidth over a 20mm on-chip serial link without any equalization. This approach offers a six times improvement in delay and 85% reduction in power consumption over a conventional RC wire with repeated buffers.

1 Introduction

Interconnects, especially the global interconnects, have been widely recognized as the dominating factor in deciding the system performance and power consumption. With ever increasing clock frequency, the inverter repeated wires can no longer keep pace with advances in transistor speed at a satisfactory cost of power consumption [7]. In order to break this "interconnect wall", many innovative interconnect technologies, ranging from optical interconnect [9] to on-chip RF communication [3], have been proposed by various research groups.

Due to the cost and design complexity considerations, the electrical signaling over on-chip transmission lines is one of the most attractive solutions for high performance on-chip communications [2]. Comparing with traditional inverter repeated RC wires, the transmission line has two main advantages. First, the signal propagates at the speed of light on a transmission line. It can achieve higher throughput at lower latency. Second, the transmission line signaling has much smaller power consumption because it eliminates the forced swing of wire capacitance in the RC wires with repeated repeaters.

One challenge to the implementation of transmission line for on-chip communication is resistive nature of on-chip metal wires. The high wire resistance causes significant frequency dependency on both wave propagation speed and attenuation. For a random digital sequence, the spectrum of the signal waveform spans a wide range. The signal phase velocity and attenuation change substantially in the operational frequencies [4]. This phenomenon renders excessive dispersion at the receiver. Inter-symbol interference (ISI) causes significant data-dependent jitter and limits communication throughput.

In order to control the waveform dispersion, several innovative approaches have been proposed. In [6], pre-emphasizing and de-emphasizing along with data aliasing are used to modulate the input wave form. In [1], Afshari and Hajimiri adopted a non-linear transmission line approach to generate solitary wave propagation and thus compensate for the dispersion. In [4], a high frequency carrier modulates the input waveform and shifts the spectrum of transmitted signal to a less frequency sensitive region. In [8], a clocked discharging scheme is adopted to erase the data dependant delay variations. In [11], an adaptive equalization scheme is used to compensate the propagation loss.

In this paper, we present a new on-chip electrical signaling scheme using distortionless transmission line. With intentionally inserted leakage conductance, the wave can preserve its original form and propagates at the speed of light, independent of its frequency. We name this scheme *Surfliner* because the way we discretely insert shunt conductors between two parallel

wiring tracks resembles the look of rail road[1]. The concept of distortionless transmission line was first proposed by O. Heaviside in 1887 [13]. The original idea is to introduce some intentional leakage on the long-distance telegraph cable, such that the wave form can be easily distinguished at the receiver's end with the fidelity to its original shape but smaller amplitude. Through careful mathematical derivation, we shall see that with exactly matched $RLGC$ values, the waveform can be transmitted without any distortion in shape along the transmission line.

We show the feasibility of the implementation of Surfliner on silicon for speed of light global communications. By periodically inserting leakage resistors between two wires of a differential pair, we can achieve near distortionless wave propagation. Experimental results suggest that: 1) At 15Gbit/s data rate, the jitter caused by the communication over a 2cm long transmission line is lower than 10ps; 2) The average power consumption of a data transportation through a 2cm long distance can be as low as 3.1pJ/bit; and, 3) The wiring channel requires less than $1000um^2$ area on poly for a 2cm long serial link.

Comparing with other schemes, the Surfliner has the following advantages:

- The signal propagation on the Surfliner is exactly the speed of light in the dielectric. This property is attractive for the connections with extreme requirement on the signal latency, for example, the global control signal in a large processor or the global data communication in a large network-on-chip.

- The waveform remains undistorted at the receiver end, and there is no ISI. As a result, the transmission produces extremely low jitter. This property enables very high bandwidth communications.

- Because the signal does not take full swing on the entire wire and no buffer is inserted, the power consumption is much less than the RC wires with repeaters.

- The scheme requires very simple sender and receiver circuits

- There are no active components between the sender and the receiver. The system is robust against process, voltage and temperature variations.

[1] *Surfliner* is the name of railroad runs between San Diego and San Luis Obispo

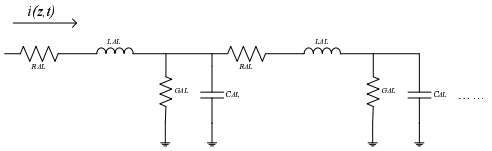

Figure 1. $RLGC$ model of a transmission line

The rest of the paper is organized as follows. In Section 2, we review the theory of distortionless transmission line. In Section 3, we describe how to exploit the distortionless transmission line for on-chip communications. In Section 4, we show the simulation results of our proposed design. At last, we conclude our paper in Section 5.

2 Theory of Distortionless Transmission Lines

In this section, we review the theory behind the distortionless transmission line. Fig. 1 illustrates a discrete $RLGC$ transmission line circuit model. Where, R, L, G, C are the unit-length resistance, inductance, capacitance, and conductance, respectively[2]. The wave is described as a function of distance, z, and time, t, by the Telegrapher's equations:

$$\frac{dV(z,t)}{dz} = -RI(z,t) - L\frac{dI(z,t)}{dt} \tag{1}$$

$$\frac{dI(z,t)}{dz} = -C\frac{dV(z,t)}{dt} - GV(z,t) \tag{2}$$

For a sinusoidal signal of angular frequency ω, the propagation of the incident wave along the transmission line can be expressed as:

$$V(z) = V_0 e^{-\alpha z - j\beta z} \tag{3}$$

where, α and $j\beta$ are the real and imaginary part of the propagation function γ, respectively, i.e.

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta, \tag{4}$$

From equation (3) we see that the exponential, $e^{-\alpha}$, of the real part of the propagation function represents the unit distance attenuation of the transmission line. The imaginary part, β, of the propagation function corresponds to the phase shift of the waves along the distance. The phase velocity of the incident wave is ω/β.

[2] Here, we assume that R, L, G, C are frequency independent constants. We shall see later in our simulation results that the jitter caused by the frequency dependency of R, L, G, C value is not significant for on-chip interconnect.

2.1 Distortion and ISI

Because silicon dioxide is a very good insulator, there is no leakage conductance, i.e. $G = 0$, for on-chip transmission lines. The real part, α, and imaginary part, β, of the propagation function can be written as equations (5) and (6). The attenuation, α, and phase velocity, ω/β, both depend on frequency ω, especially when the wire resistance, R, is comparable to or larger than the impedance ωL contributed by wire inductance.

$$\alpha = \sqrt{\frac{1}{2}}\sqrt{-\omega^2 LC + \omega C\sqrt{\omega^2 L^2 + R^2}} \tag{5}$$

$$\beta = \sqrt{\frac{1}{2}}\sqrt{\omega^2 LC + \omega C\sqrt{\omega^2 L^2 + R^2}} \tag{6}$$

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2.2 Distortionless Transmission Line

We design a transmission line by inserting leakage conductance. The shunt conductance provides an additional current path to compensate for the voltage drop due to serial resistance. The attenuation still exists, but becomes frequency independent. In other words, the effects of the series resistor and shunt conductance cancel out so that the waves propagate without distortion. The net effect is that the signal can now move at the speed of light in the media.

We set the leakage conductance G per unit-length as the following equation.

$$G = RC/L \tag{7}$$

Substituting equation (7) in equation (4), we get the *frequency independent* attenuation and phase velocity, i.e. distortionless transmission.

$$\alpha = R/\sqrt{L/C} \tag{8}$$

$$\beta = \omega\sqrt{LC} \tag{9}$$

For this distortionless transmission line, we obtain the following.

Characteristic impedance:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{10}$$

Phase velocity:

$$v = \frac{1}{\sqrt{LC}} = c \tag{11}$$

Attenuation:

$$A(z) = e^{-\frac{R}{Z_0}z} \tag{12}$$

The distortionless transmission line has pure resistive characteristic impedance (8). The attenuation is an exponential function of the ratio between wire resistance and characteristic impedance, i.e. $e^{-\frac{R}{Z_o}}$. The phase velocity is exactly the speed of light in the dielectrics, $\frac{1}{\sqrt{LC}}$. Both the attenuation and the velocity are independent of frequency. There is no distortion on the signal waves from direct current (DC) mode to very high frequency as long as the $RLCG$ values remain the same.

For typical on-chip transmission line implemented on upper low impedance metal layers, the resistance of a several micron wide wire can be less than 10ohm/mm, and the differential characteristic impedance of transmission lines is usually around 100ohm. Thus, an input signal with magnitude of 1.0V will have a magnitude of 135mV after traveling a distance of 2cm.The state-of-art sense amplifier can easily detect the output signal at this magnitude. [10]

Fig. 2 illustrates the characteristics of a differential pair of $2cm$-length and $4\mu m$-width wires. We observe significant changes in attenuation and phase velocity (Fig. 2(a)). When shunt conductance $G = 0$, the attenuation ranges from 0.9997 at 1KHz to 0.644 at 1GHz. Note that there is no voltage magnitude drop when the attenuation value is 1. The phase velocity ranges from $9.0\times10^7 mm/s$ at $1KHz$ to $8.5\times10^{10} mm/s$ at 1GHz. The curve saturates at the speed of light in dielectric $1.8 \times 10^{11} mm/s$ when the frequency is above 1THz. For our proposed distortionless pairs, the attenuation is 0.4147 and the phase velocity is at the speed of light. The curves of the distortionless wires are flat.

Fig. 2 (b) shows the dispersion in time domain. The input is the square wave at left, which rises at 50ps. When shunt conductance $G = 0$, the output disperses on the rising and falling edges. There is a very long tail at the falling edge, which can interfere with the following input bits unless we wait until the wave drops below some threshold. This intersymbol interference is one limiting factor of the performance of the transmission lines.

For the distortionless pairs, the magnitude of the signal drops. The rising edge starts at 161ps, the same rising time as the wires with no shunts. However, the output maintains a square waveform. The delay is $161 - 50 = 111ps$, which is at the speed of light, $1.8 \times 10^{11} mm/s$ for $2cm$ length.

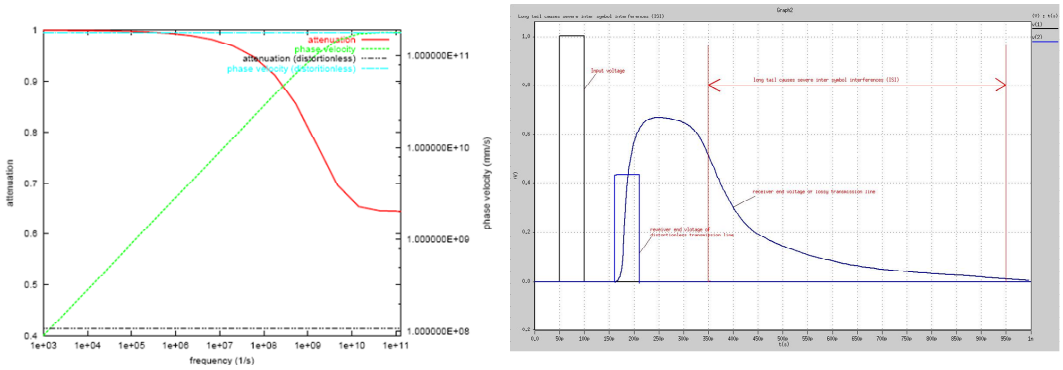

Figure 2. The attenuation and phase velocity v.s. frequency for a on-chip wire

2.3 Sensitivity of Distortionless Transmission Lines to the Parameters Variations

One nice property of the distortionless transmission line is that it is much less sensitive to the process, voltage, and temperature variations than traditional interconnects. First, the speed of light is determined by the dielectric constant. The feature size variations do not significantly affect the speed. Second, in the following, we show that distortionless wires are designed to minimize the sensitivity of the wire resistance and shunt conductance variations.

We observe the sensitivity due to shunt conductance variations. The derivation of the sensitivity due to wire resistance changes is similar. Assume that the leakage conductance G varies from its perfectly matched value RC/L by a constant factor Δ, i.e. $G = (1+\Delta)RC/L$. Substituting this expression into equations (5) and (6), using Taylor's expansion, we derive the attenuation constant and phase velocity in the second order.

$$\alpha = \frac{R}{\sqrt{L/C}}(1 + \frac{1}{2}\Delta - \frac{1}{8}\frac{R^2}{R^2+\omega^2L^2}\Delta^2) \qquad (13)$$

$$v = \frac{1}{\sqrt{LC}}(1 - \frac{1}{8}\frac{R^2}{R^2+\omega^2L^2}\Delta^2) \qquad (14)$$

In equations (13) and (14), the frequency dependent terms occur not at the first but the second order. Note that for the attenuation constant, we have a first order term independent of the frequency. In other words, this first order term does not contribute to the distortion. For the phase velocity, the first order term is zero. Therefore, we can derive that the shunt conductance $G = RC/L$ is the solution to minimize the skew sensitivity. Applying a similar procedure, we can also derive that given the shunt conductance $G = RC/L$, the serial resistance R is the solution to minimize the skew sensitivity.

The coefficients of the second order terms in equation (13) and equation (14) are limited by an upper bound $\frac{1}{8}$. Suppose that the shunt conductance changes by ten percent, i.e. $\Delta = 0.1$. We can derive that the third order terms in equations (13) and (14) deviate by no more than $\Delta^2/8 \approx 0.0012$.

3 Exploiting the Surfliner for On-Chip Communications

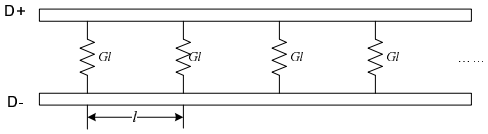

Figure 3. On-Chip Implementation of Surfliner

For Surfliner, we insert the resistors between two wires of a differential pair to realize the leakage conductance G (Fig. 3). We periodically insert a leakage conductor with conductance Gl at every interval l in z direction. When the interval l is small enough comparing with the wavelength of the data signal, the discontinuity caused by this discrete resistor insertion scheme is negligible. According to our simulation, when interval $l < \frac{c}{20}t_p$, the jitter caused by ISI is smaller than 5% of clock period, t_p, where, c is the speed-of-light in the dielectrics. For a 15GHz signal, we need to keep the interval l to be smaller than $600\mu m$.

The leakage resistor can be implemented using either unsilicided poly resistor or diffusion resistor (Fig. 4). In our implementation, we choose unsilicided poly resistor because it occupies less area. The sheet resistance of unsilicided poly can be as high as

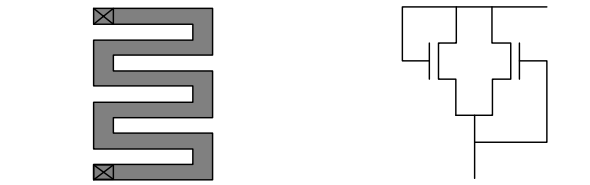

Figure 4. Design of shunt conductors

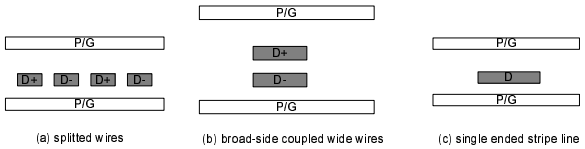

Figure 5. Wire configurations to increase the coupling between differential wires

1000ohm/square. We assume 90nm technology, a 3um-width copper wire at metal 6, and 500ohm/square sheet resistance of unsilicided poly. If we insert a leakage resistor every 200um and implement each resistor using poly wires with minimal width (100nm), for a 20mm long link, the leakage conductors only use $126um^2$ of poly area.

For Surfliner, because the attenuation of the signal is proportional to the exponential of the ratio between wire resistance and characteristic impedance, reducing the wire resistance as well as increasing the transmission line characteristic impedance are important to reduce the attenuation. Reducing attenuation can benefit the simplicity of the receiver, the power consumption of the system, and the robustness against the crosstalk and other variations. Different wire configurations, such as the split wires (Fig. 5(a)), broad-side coupled wide wires (Fig. 5(b)), and single ended stripe lines (Fig. 5(c)), can be adopted to optimize under different design specs.

4 Simulation Results

We implement the surfliner using a pair of edge-coupled stripelines (Fig. 6). The copper wires reside on the low resistive upper metal layers, where the wire thickness is $1um$. Each wire has a width of $4um$ and the separation between the wires is also $4um$. The wires are sandwiched by a pair of power/ground shields with separation of $1.5um$. The shields above and below the wires runs in parallel with the wires.

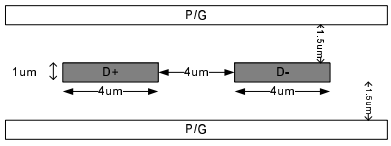

Figure 6. Implementation of Wires

We extract the per unit length resistance, inductance, and capacitance values, R, L, C, of wires using FastHenry and FastCap. In our design, at $15GHz$, $R = 4.4\Omega/mm$, $L = 0.44nH/mm$, and $C = 196.418fF/mm$, the characteristic impedance of the differential pair is $84.5 \times 2 = 169\Omega$. We define the segment of each inserted shunt conductor a stages. We change the number of stages from 4 to 200. For a pair of 2cm long wires, for the distortionless pair, the total leakage conductance is $6.15 \times 10^{-4}S$. The resistance of each resistor ranges from $6.5k\Omega$ to $325k\Omega$. Assuming 1.0V swing level at the output of the sender, the signal amplitude at the input of the receivers is 365mV.

Table 1. Jitter and silicon area usage

# Stages	4	10	20	40	80	120	160
Jitter(ps)	27	9.5	5.4	4.2	3.9	2.1	2.08
Area(um^2)	0.52	3.25	13.0	52	208	468	832

For each stage, we use Agilent ADS Momentum to extract the 4-port S-parameter description. Then, we perform the transient analysis of the circuit using HSpice. We generate $2^{10} - 1 = 1023$ bits pseudo random bit sequences (PRBS) as the input [12]. The initial bit vector of PRBS is 1010101, and the generation polynomial is $x^7 + x + 1$. We set the clock frequency to 15GHz, and the input signal has a transition slope of 10% clock cycle for each rising and falling edge.

We simulate surfliners with different numbers of leakage resistors. Table 1 shows the jitter of output voltages and the usage of poly area. When the number of stages increases from 4 to 160, the jitter reduces from 27ps to 2.08ps. The poly area usage increases from $0.52um^2$ to $832um^2$.

Figs. 7 and 8 show the eye diagrams of the output signal for surfliners with 4 stages and 120 stages, respectively. Both of the cases show clear eye opening. For 4-stage case, we see jitters caused by reflections.

Table 2. power consumption w/ different wire width and sepeartion

(width, spacing (um))	(3, 3)	(4, 4)	(5, 4)	(10, 5)
Power (mW)	4.98	3.62	3.02	2.13
Attenuation	0.307	0.415	0.496	0.60

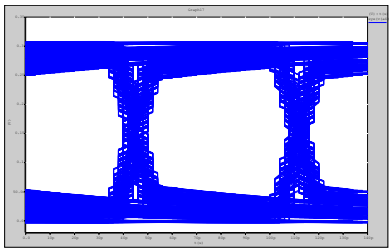

Figure 7. Eye diagram of the output voltage for a 4 stage 2cm-length surfliner

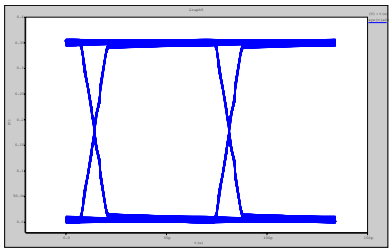

Figure 8. Eye diagram of the output voltage for a 120 stage 2cm-length surfliner

(Fig. 7). For 120-stage case (Fig. 8, the transmission line achieves almost distortionless transportation. The data dependent jitter is only 2.1ps.

We also explore the effect of different configurations of wire geometries. Table 2 shows the power consumption and signal attenuation through a 2cm long transmission line with different wire widths and separations. The driver is designed to ensure that the signal magnitude at the receiver end is no less than 150mV. The wires are terminated at the receiver ends. When we use wider wires, we can get lower attenuation. As a result, the wider wire requires less power consumption.

5 Conclusion

We propose a novel scheme to implement a distortionless transmission line for on-chip global communications. By inserting shunt conductors between two wires of a differential pair, we can achieve near distortionless wave propagations. Our on-going efforts include: (1) Design and fabrication of test chip for this new architecture. (2) Implement and evaluate wiring splitting schemes shown in Fig. 5. (3) Investigate novel on-chip interconnect architectures which exploit unique advantages of distortionless transmission lines to realize low-latency low-power on-chip communications.

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