Inexpensive Student-Assembled FPGA / Microcontroller Board

Sarah Harris and David Harris
Department of Engineering
Harvey Mudd College
Claremont, CA 91711
{Sarah_Harris, David_Harris}@hmc.edu

Abstract

Digital design courses need evaluation boards to mount FPGAs or microcontrollers and the appropriate support circuitry. These boards can be costly to purchase and maintain. Harvey Mudd College has developed a series of inexpensive evaluation boards for an embedded systems laboratory class that are assembled and maintained by the students in the class.

1. Introduction

For the past six years, Harvey Mudd College has used three generations of evaluation boards for projects with FPGAs and microcontrollers in an embedded systems laboratory (E155). Students purchase a lab kit for $50 containing a bare printed circuit board (PCB) and components. At the beginning of the semester, they learn to solder, then assemble and debug their own board. They proceed to undertake a sequence of laboratory assignments culminating in a team final project to build a system of the students' choosing. This paper describes the evolution of the evaluation board and the lessons we have learned.

2. Evaluation Board Features

The main requirements for the evaluation board are:

- hosts microcontroller and FPGA
- provides clock (single-steppable), LEDs, switches
- interfaces easily with a breadboard
- easy for students to assemble and maintain
- inexpensive for students to purchase

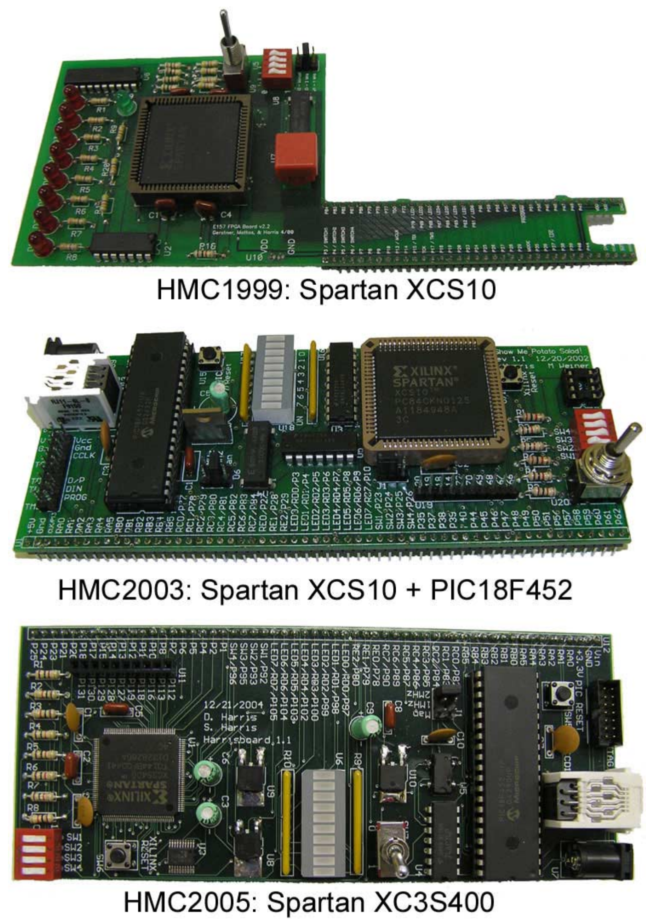

Fig. 1. Three generations of FPGA / microcontroller boards

Commercially available evaluation boards typically retail for $99 or more, and they come preassembled. Students, however, have consistently reported enjoying the experience of learning to solder and assemble their own board. Moreover, they have an easier time troubleshooting problems on a board that they have assembled themselves.

The three generations of boards are shown in Fig. 1. All of the boards contain LEDs, DIP switches, header pins to plug into a breadboard, and a clock system with a jumper to select a debounced single-step clock. Undergraduates participated in designing, building, and testing the boards and porting laboratory projects.

The first generation HMC1999 board was built around the XCS10 Xilinx Spartan FPGA with approximately 10,000 equivalent gate capacity. It connected to a breadboard through two rows of header pins. The 84-pin PLCC FPGA package mounted easily in a through-hole socket so no surface mount (SMT) assembly was necessary. A 2 MHz oscillator was provided. A Motorola

68HC11 microcontroller evaluation board hosted the microcontroller and connected to the breadboard through a ribbon cable and jumper wires. The design had several limitations. The HC11 evaluation boards were easily damaged by inexperienced students and replacement boards were discontinued. The jumper wires easily fell out of the ribbon cable. And the two rows of header pins were cute but difficult to insert and remove from the breadboard.

A second generation HMC2003 introduced a single-chip microcontroller. From among many good choices, the PIC18F452 was selected because it is widely used, well-supported, and inexpensive. The header pins were moved into a single row for easier connectivity. Unfortunately, the XCS10 FPGA has become obsolete. Xilinx presently ships ISE 6.3i development tools, while the last release that supports the XCS10 was 4.2i. The schematic editor in 4.2i is incompatible with the XCS10, so the introductory digital design course (E85) could not implement schematic-level designs onto the board.

We are now using a third generation HMC2005 board that upgrades to a XC3S400 Xilinx Spartan 3 FPGA with 400,000 equivalent gate capacity, 288 Kb embedded RAM, 16 dedicated multipliers, and digital clock management. The oscillator is bumped up to 40 MHz, requiring a 4-layer board with dedicated supply planes and better decoupling. To maintain signal integrity, this fast clock must be divided down before it is driven onto the highly capacitive breadboard. The new chip will provide students with a state-of-the-art FPGA, support the latest tools and the schematic editor, and postpone obsolescence. Unfortunately, the FPGA and its configuration EEPROM are only available in fine-pitch (20 mil) surface mount packages (TQFP144 and VO20, respectively). At the time of this writing, we have been unable to find a technique for novices to reliably solder the SMT packages to the board. We provide the boards with these two chips preassembled by a technician.

3. Lab Assignments

Table 1 lists the E155 laboratory assignments using the evaluation boards. Assembling and testing the board each typically require four hours for an inexperienced student. Students add a multiplexed dual seven-segment display and keypad as they learn to interface with the external world.

Labs are done individually and require on average nine hours of work per week. During check-off, the instructor asks a *fault-tolerance question* for each student. A typical question asks how the system would behave differently, if at all, if something were changed. For example, the two legs of a bypass capacitor might be shorted, an LED might be inserted backward, or an incorrect resistor might be used. Students can consult inanimate resources to prepare their answer, but must not test their theory until they are ready to complete the check-off. Students enjoy the challenge of fault tolerance questions and often understand their boards more deeply after contemplating why each component is necessary.

Lab	Description
1	Intro to Verilog. 7-segment display decoder
2	Assemble and test evaluation board
3	Multiplexed 7-segement display
4	Keypad
5	Intro to PIC assembly, sorting
6	Traffic light controller
7	Pulse-width modulation

Table 1. E155 laboratory assignments

The semester ends with a five-week final project done in teams of two. Projects must use the FPGA and microcontroller and perform an interesting function of the students' own choosing. Projects have included an inverted pendulum, a light-avoiding robot, an RF-to-infrared remote control with error correction, and many video games [1].

4. Software

The HMC1999 board used Xilinx ISE 2.1 and the Buffalo monitor for the 68HC11. ISE bugs were a major complaint from the students and the Verilog synthesis tools did not produce schematics of the hardware implied. FPGA configuration files were burned into an EEPROM using a dedicated programmer.

The HMC2003 board moved to Xilinx ISE 4.2i with Synplicity Synplify Pro for synthesis and Mentor Graphics Modelsim for simulation. These third-party tools are much more robust and are inexpensive through university programs. Synplify displays schematics of the synthesized logic, helping students relate HDL to gates. The FPGA could be configured from the EEPROM or through the Xilinx Parallel Cable IV. The PIC was programmed through Microchip's integrated development environment (IDE) over an in-circuit debugger (ICD). Microchip IDE is surprisingly unstable and has become more so in the 2004 release; this is now the major source of student complaints.

The HMC2005 board is programmed from Xilinx ISE 6.3i with Synplify Pro and Modelsim. The EEPROM is programmed via JTAG over the Xilinx Parallel Cable IV so no separate programmer is necessary. E85 students will now experiment with simple digital designs using the schematic editor and a pre-assembled evaluation board. The PIC environment is unchanged.

5. Conclusions

Students enjoy the full experience of building from a bare SMT printed circuit board to a sophisticated final project. The open-source HMC2005 PCB files and bill of materials are freely available at [2].

References

[1] http://www3.hmc.edu/~harris/class/e155/
[2] http://www3.hmc.edu/~sharris/Board/