The Microprocessor as a Microcosm:

A Hands-On Approach to VLSI Design Education

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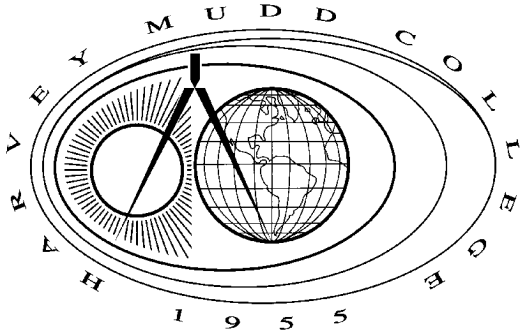


Outline

- Introduction
- Course Organization
- CAD
- Laboratories
- Projects
- Testing
- Assessment
- Conclusion

Introduction

Changing face of Very Large Scale Integration (VLSI) design education

Level of instruction

- Primarily graduate-level in early 1990's
- Transition to junior/senior level elective

Maturing design tools and methods

- Move in industry from custom layout to synthesized designs
- Yet still a strong need to understand fundamentals from the mask level

Project-based VLSI Education

- Best way to understand VLSI design is to design and build a chip
- Also plays role as major team design experience for undergraduates

Instructor-Defined vs. Student-Defined Projects

- Instructor-defined projects allow more guidance in good design practices
- But students mature more by taking a project from definition to completion
- This paper describes an approach seeking the best of both worlds
- Series of 5 labs to build an 8-bit microprocessor followed by team projects
- Microprocessor serves as microcosm to illustrate larger design issues
- Relates back to computer engineering class and is highly motivational

Course Organization

E158: Introduction to CMOS VLSI Design

Enrollment:

- Mostly junior and senior Engineering majors (60 in each senior class)
- A few from CS, Physics, and Chemistry
- Spring 2001: 42 enrolled, 9 dropped
- Spring 2002: 15 enrolled, 0 dropped (conflicted with required class)

Prerequisites:

- E84: Introduction to Electrical Engineering
- E85: Introduction to Computer Engineering

Textbooks

- Weste & Eshraghian: *Principles of CMOS VLSI Design*
- Sutherland, Sproull, & Harris: *Logical Effort*
- Harris: *Skew-Tolerant Circuit Design*

Schedule: MW 2:45-4:00

Credit: 3 units

Grading: 40% labs, 45% project, 10% problem sets, 5% in-class activities

Spring 2002 Schedule

Date	Topic	Due
23 Jan	*Introduction & overview*	
28 Jan	*Circuits, fab, layout*	
30 Jan	*Microprocessor example*	Lab 1: Gate Design
4 Feb	*-- ISSCC: No Class --*	PS1
6 Feb	*CMOS transistor theory*	Lab 2: Full Adder Design
11 Feb	*DC gate characteristics*	
13 Feb	*CMOS processing*	Lab 3: Datapath & Zipper Assembly
18 Feb	*Logical effort*	PS2
20 Feb	*Interconnect*	Lab 4: Synthesized Controller
25 Feb	*Simulation*	Preliminary proposal
27 Feb	*Combinational circuits*	Lab 5: Chip Assembly
4 Mar	*Circuit Families*	Final proposal
6 Mar	*Sequential circuits*	
11 Mar	*Adders*	PS3
13 Mar	*Datapath functional units*	Floorplan

Schedule (continued)

Date	Topic	Due
18 Mar	*-- Spring Break: No Class --*	
20 Mar	*-- Spring Break: No Class --*	
25 Mar	*Memories I*	
27 Mar	*Memories II*	Schematics complete
1 Apr	*Control system design*	PS4
3 Apr	*Design for test*	
8 Apr	*In class design reviews*	Leaf cells complete
10 Apr	*In class design reviews*	
15 Apr	*Power & clock distribution*	
17 Apr	*Skew-tolerant circuits*	Final project & report
22 Apr	*Asynchronous design*	
24 Apr	*Low power design*	PS5
29 Apr	*Scaling & economics*	
3 May	*Microprocessor slideshow*	PS6
6 May	*Presentation Day*	Project presentations

CAD

VLSI CAD tools are an issue for a small teaching college

- Computer labs are primarily Windows, limited Solaris servers
- Cadence & Mentor Tools are very time-consuming to maintain
- Tanner Tools are less powerful and relatively expensive
- Magic has clumsy interface and is primarily available on Unix

Seminar has used the Electric CAD system

- Open source free CAD system
- Developed by Dr. Steve Rubin at Sun Microsystems Laboratories
- Schematics, layout, simulation, DRC, LVS, ERC capabilities
- Support Windows, Solaris, Macintosh
- Required close work with Dr. Rubin to improve tools
  - 397 bug / feature enhancement reports since Spring 2000
  - Over 350 of these have been addressed
  - Often next-day response!
- Tools are now reasonably stable
  - Nine chips successfully fabricated in 1.5 and 0.6µ processes

Synopsys Design Analyzer for HDL synthesis

Laboratories

Objectives:

- CAD tool tutorial:
  - schematics, icons, layout
  - switch-level simulation (IRSIM)
  - synthesis & place & route
  - Design Rule Checker (DRC)
  - Electrical Rule Checker (ERC)
  - Network Consistency Check (NCC, aka LVS)
- Illustrate good design practices
  - design of a complex system: regularity, modularity, hierarchy
  - datapath, control, memory
  - methodical verification

Lab overview:

- Implement 8-bit subset of MIPS processor (from Hennessy & Patterson)
- Building a processor from scratch takes the entire semester, is repetitive
- Students begin with library with much of the processor
- Complete one of each interesting type of component on their own
- Work in campus computer labs or from home PCs

Lab Assignments

Lab 1: Gate design

- Guided through schematics, icon, & layout of datapath NAND2 & AND2
- Learn simulation, DRC, ERC, NCC, hierarchy
- Independently design NOR2 and OR2

Lab 2: Full adder design

- Open-ended design & test of datapath full adder cell, optimizing for size

Lab 3: Datapath & zipper assembly

- Combine AND2, OR2, FULLADDER with provided mux to build ALU
- Attach ALU to datapath bitslice & add mux select drivers to zipper

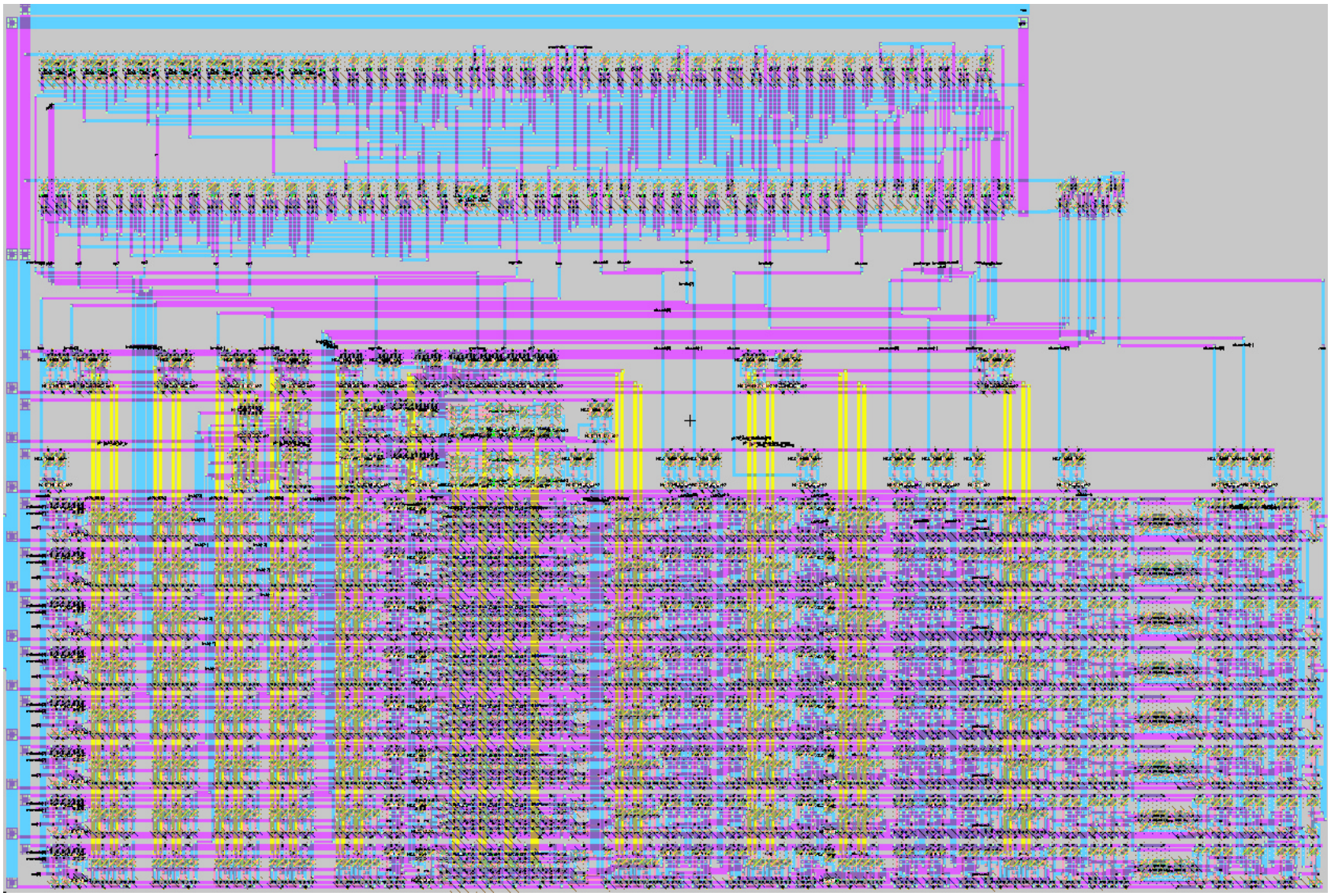
Lab 4: Controller design

- Layout standard cell NOR3
- Manual design & layout of ALUCONTROL using standard cells
- Modify Verilog model of CONTROLLER to support ADDI instruction
- Synthesis, place & route

Lab 5: Microprocessor assembly

- Full chip assembly, pad frame, test vector generation
- CIF out & tapeout checks

MIPS Processor Layout



Projects

Objectives:

- Major team design experience (groups of 2)
- Take VLSI system from specification through tapeout
- Teamwork & leadership
- Technical documentation, design review, & presentation practice
- Emphasize management of complexy rather than heavily optimizng circuits

Schedule:

- Tapeout before clinic consumes last weeks of students' attention
- Work expands to fill time available so milestones are strictly enforced
- Milestones
  - Preliminary Proposal
  - Final Proposal
  - Floorplan
  - Schematics Complete
  - Leaf Cells Complete
  - Design Review
  - Project Complete
  - Formal Presentation

Fabrication

Projects target MOSIS TinyChip

- AMI 0.6μm 3-level metal process
- 1.5 x 1.5 mm^2 die in 40-pin DIP
- 3400 x 3400 λ of core area excluding padframe

MOSIS / Semiconductor Industry Association Fabrication Grants

- Support fabrication of 3-4 projects / semester
- Team must include a junior who commits to testing the chip in the fall

Testing

Testing on breadboards used to take students all semester

Now use TestosterICs chip tester built at HMC

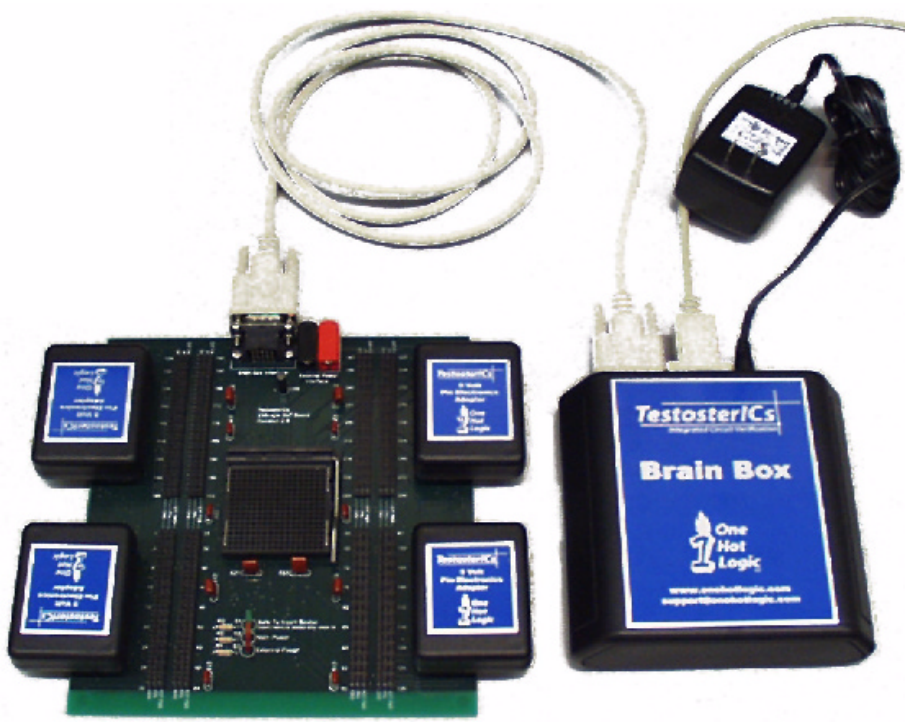
- Low speed functional testing
- Reads IRSIM vectors from pretapeout test
- 45 minutes to learn tester and test chips
- www.onehotlogic.com

2001 Test results

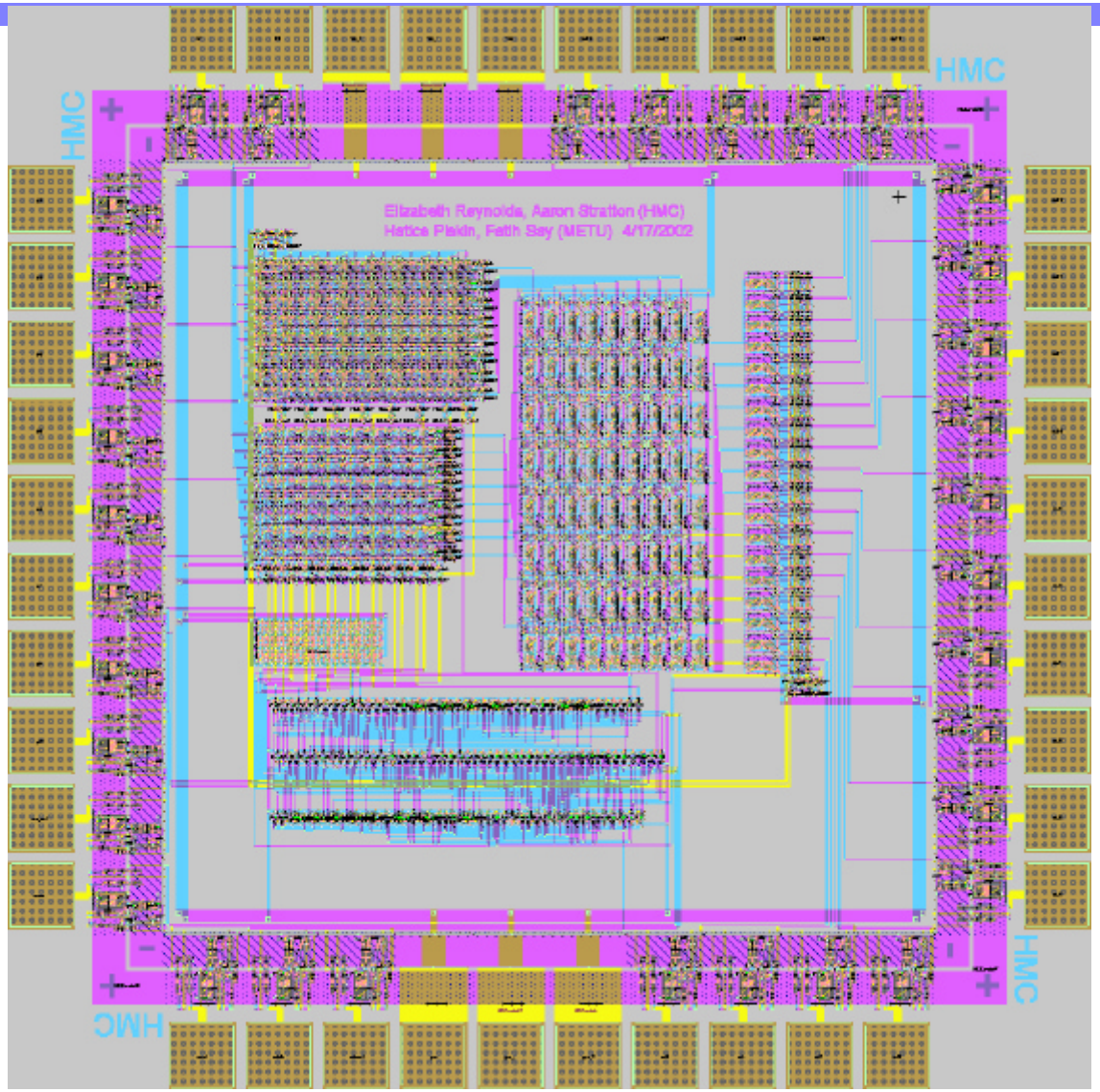
- 1 chip fully operational
- 3 chips had opens or shorts in global routing that could be worked around
- Electric extraction incompatible with old pad frame so top level had not been verified

2002 Test results

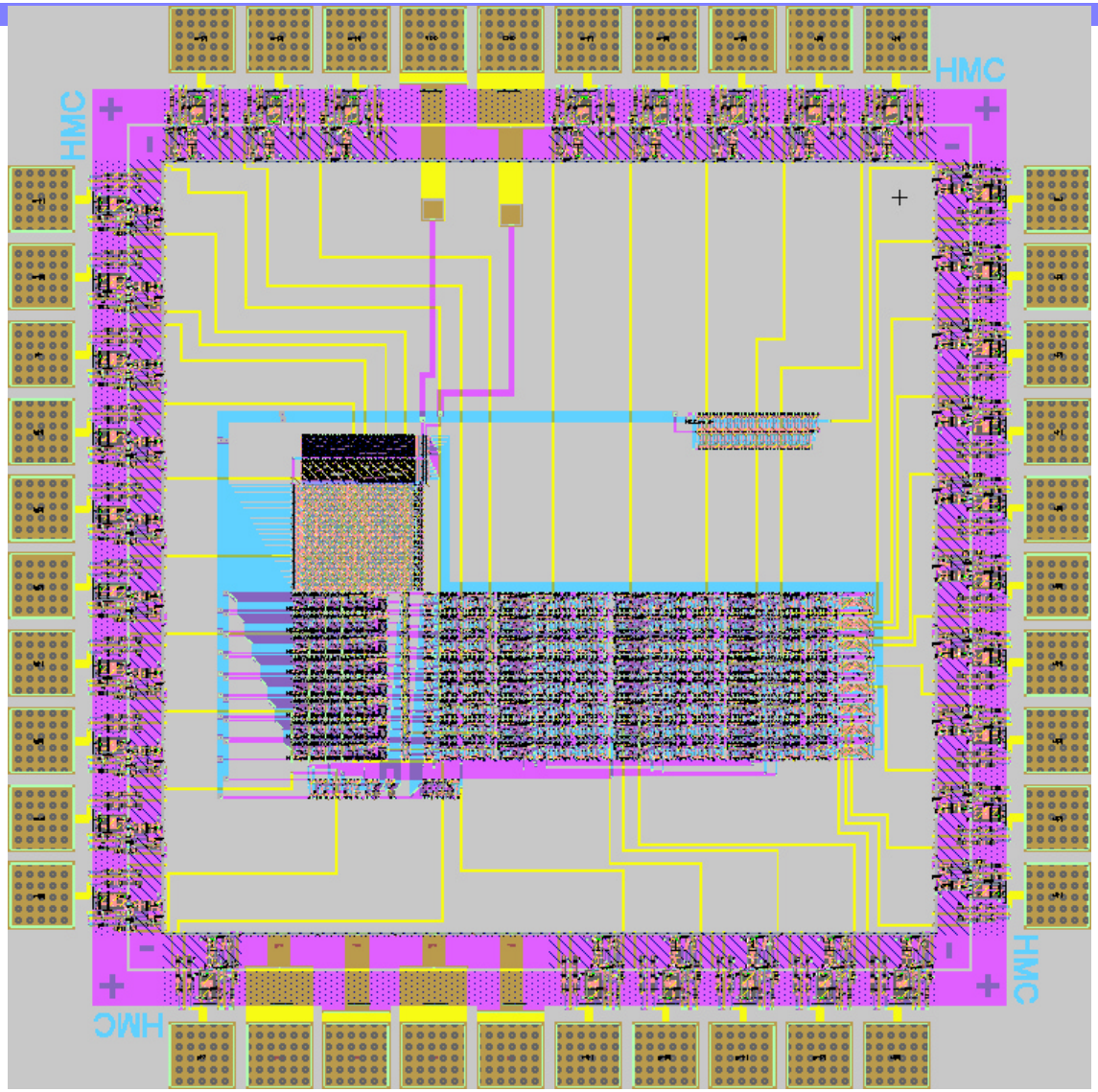
- all 3 chips fully operational



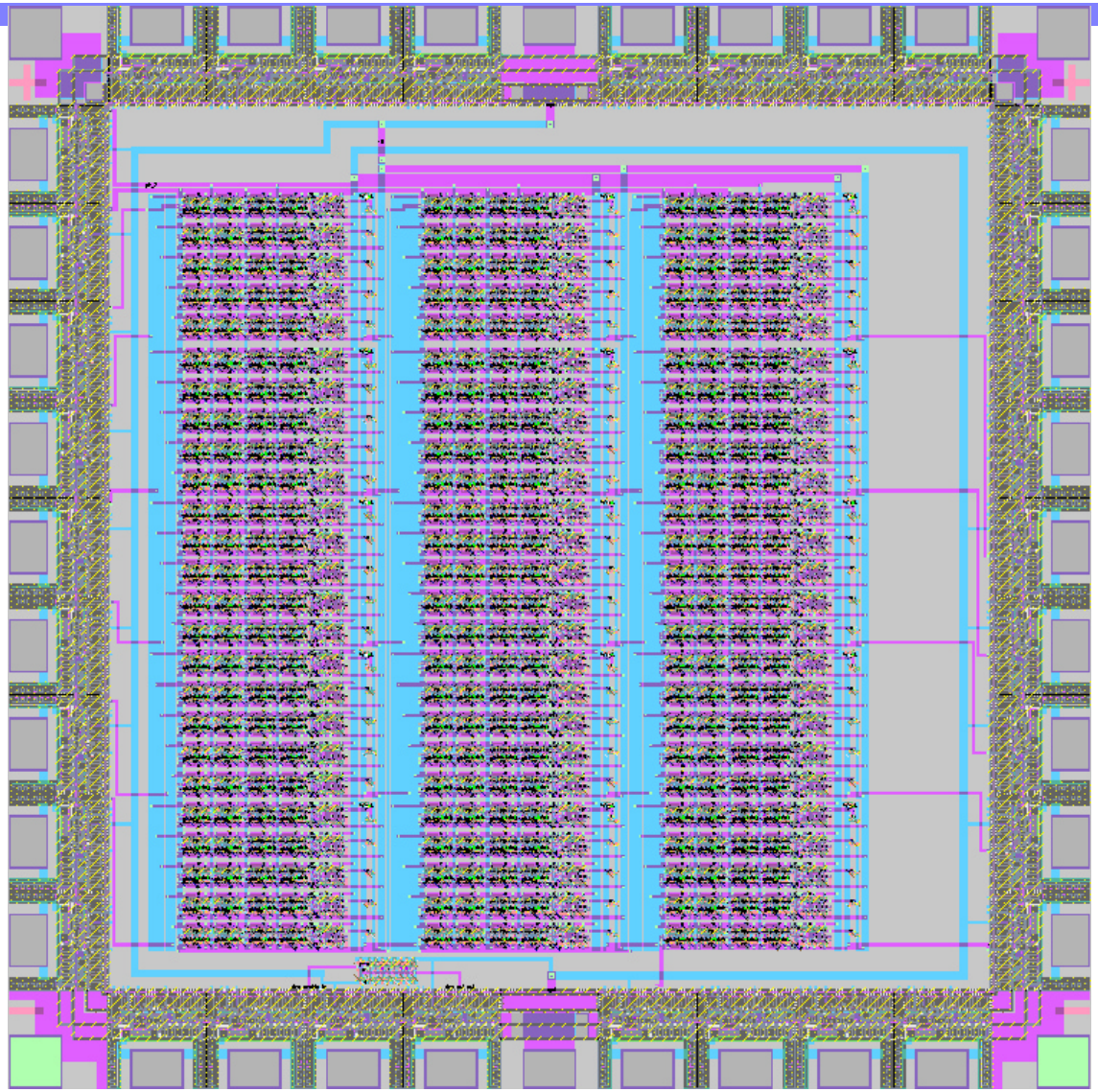
8-Bit FIR Filter



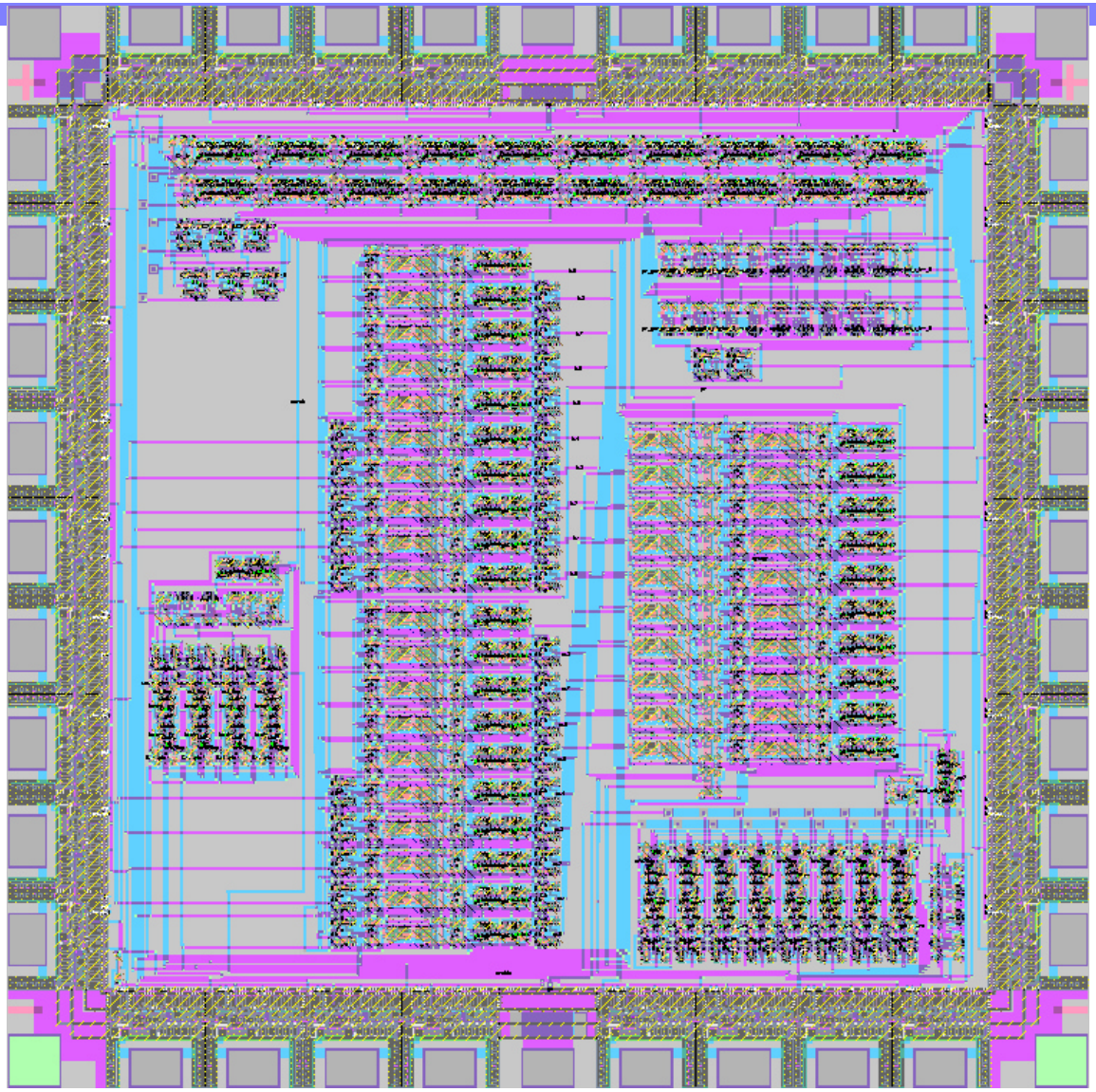
Hangman Game



Neural Network



GPS Correlator



Assessment

Hands-on VLSI design is time consuming but within reason for a 3-unit elective

- Students reported time spent on each lab

Lab 1	5.4
Lab 2	8.9
Lab 3	17.0
Lab 4	7.8
Lab 5	7.5

- Project effort varied widely, but 100 hours/team over 6 weeks was typical

Project Success

- 2001: 13 of 17 projects completed, remaining 4 showed significant effort
- 2002: 8 of 8 projects completed

Teaching Evaluations were very positive

- 6.5 - 6.6 / 7; campus average 5.8 / 7
- Students supported combination of labs and project
- “great that the class ended in early April so we didn’t have to worry about it.”
- Desire more opportunity to apply high-performance design

Conclusion

The MIPS processor labs served as a microcosm to illustrate design issues

- CAD tutorial
- Good design practices for complex systems
- Connection to prerequisite course
- Highly motivational

Most of the processor was provided and students focused on unique cells

- Reduced repetitive work
- Allowed completing microprocessor in first third of the semester
- Left time for in-depth final team projects

Class will continue to be tuned

- Split lab 3 over two weeks
- Apply more high-speed design techniques on short problem sets