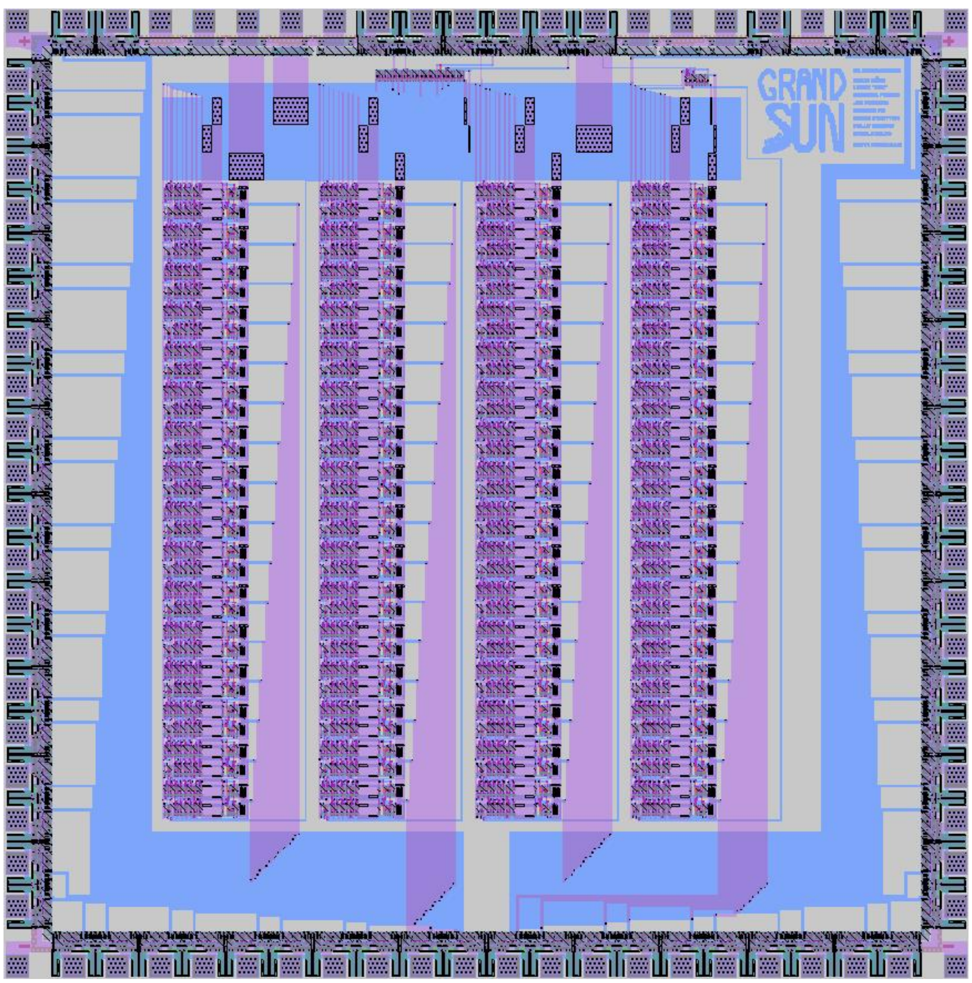
GrandSun of MacTester

Pin Electronics Chip Report

David Harris
November 15, 1999 with pin updates September 28, 2000



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Introduction

The GrandSun of MacTester is a tester being developed by the 1999-2000 Sun Microsystems Clinic Team supporting I/O voltages in the range of 1-7 volts. It improves the tester from the 1998-1999 Sun Clinic project by replacing over 100 MSI comparator and switch chips with two to four custom pin electronics chips providing data storage and input and output conversion for the device-under-test (DUT) pins.

This report documents the GrandSun of MacTester Pin Electronics chip designed by a team of freshmen in the E180C Digital Electronics and Chip Design seminar, Fall 1999. The designers include David Diaz, Lance Feagan, Romanos Fessas, Joseph Friesen, Aaron Stratton, and Molly Waring, along with sophomore Aiyesha Ma and the clinic team leader April Fields, organized by the noninvertable Dr. Harris.

The chip was constructed in the MOSIS 1.6 micron process manufactured through AMI. It uses over 7000 transistors in a 4.5 mm square die packaged in an 84 pin Pin Grid Array (PGA).

This report documents the chip specifications, the verification process used before tapeout, the electrical characterization results, the chip pinout, and the schematics and layout of each cell. Appendices include the tapout procedures and a copy of the design report from another pin electronics test chip prototyped by David Harris, Spring 1999.

Specifications

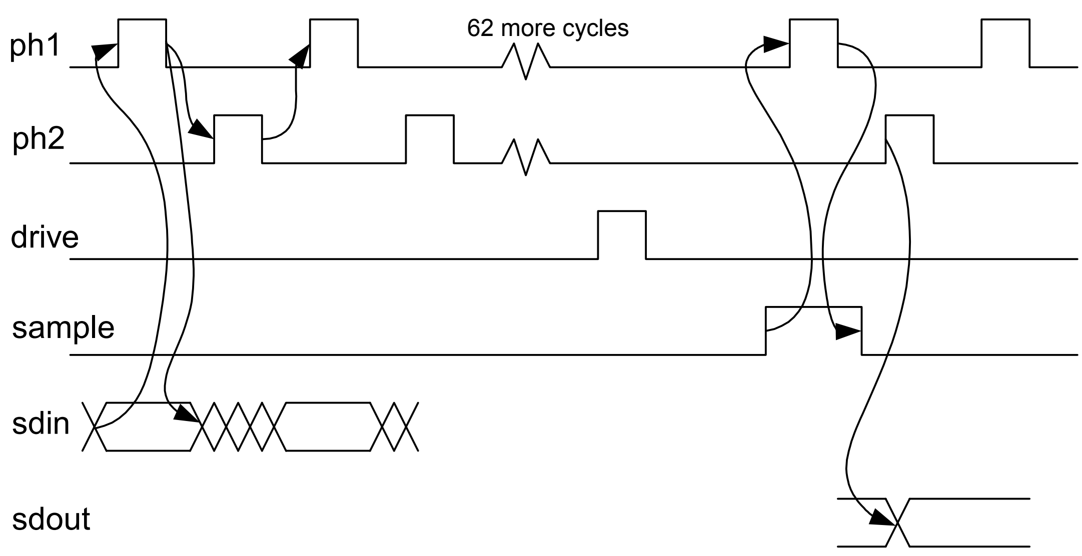
The Pin Electronics chip is responsible for controlling 64 DUT pins, each of which may be an input or an output. It consists of 64 cells, each with an enable. When the enable is true, a data value is driven to the DUT input pin. When the enable is false, the tester does not drive the DUT output pin.

The user applies a test vector by serially scanning 128 bits into the pin electronics chip, representing the 64 enables and data values. The user then pulses a drive pin to drive the DUT pins with the new values. The user may then pulse a sample pin to copy data from the DUT back into the scan chain. Finally, the user scans the 128 bits back out; half of these bits contain the data from the DUT.

The Pin Electronics chip is manufactured in the AMI 1.6 micron process and packaged in an 84 pin PGA. It has the following pins:

Inputs	Outputs	DUT Pins	Voltage Sources
ph1	sdout	p0-p63	vdd (2)
ph2			gnd (6)
sdin			vext(5)
sample			vrefovertwo
drive			

ph1 and ph2 are a two-phase non-overlapping clock used for scanning data. sdin is the scan data input. sdout is the scan data output. After scanning 128 bits, the first bit loaded controls the enable of pin 63; the second bit controls the data of pin 63, the 127th bit controls the enable of pin 0; and the 128th bit controls the data of pin 0. When drive is pulsed, latches capture the enable and data values to control the DUT pins. When sample is high and ph1 is pulsed, data is copied from the DUT pins into the scan chain. These operations are shown in the timing diagram below.



For testing purposes, there is a ring oscillator that connects to sdout when sample is asserted. The basic operation of the pads can be checked by rising sample and looking for an oscillation at about 125 MHz on sdout. This does not affect normal operation because sample is usually low, disabling the oscillator, and because the user is not concerned about the value of sdout when sample is asserted.

A copy of the desired specifications from the Sun Microsystems Clinic Team is attached in Appendix I. The edge rates and output current achieved are described in the Electrical Characterization section of this report. The actual design has one more Gnd pin and one fewer Vdd pin than requested by the clinic team. Electrostatic discharge structures from the MOSIS pad frame are provided but require testing to spec.

Verification

This section documents the verification procedure performed on the pin electronics chip.

The verification was complicated by the fact that the input converters are comparators not analyzed properly by IRSIM. Each cell in the layout passed a gemini layout-vs-schematic (LVS) test against the corresponding schematic. The generated CIF file was reloaded into magic and extracted. It was checked for DRC, LVS, SPICE, and floating well errors. The CIF file was also visually inspected for obvious problems.

The chip is not entirely DRC clean. There are errors in the input protection resistor of the input and output pads and in some wells. The input resistor diffusion came from the pads provided by MOSIS, so we considered it correct despite DRC warnings that it was too close to a substrate tap. The wells formed by the CIF generator were ragged and thus produced some DRC errors between adjacent cells. These errors went away when the cell was flattened.

Care was taken to avoid shorting the VDD and VEXT wells at the output converter and the pad ring. The output converter and DUT pads all have wells and supplies of VEXT. The remainder of the chip operates at VDD.

The chip passed LVS checks at the top level cell (core), including the I/O pads. An edit shortly before tapeout introduced an error within the oc output converter cell; d is not attached to the input inverter with metal within the cell. d is correctly connected in the next level of the layout, superscan, however, so the chip is correct.

The chip was loaded into HSPICE and floating capacitors were deleted with the rmfloat.pl script by David Diaz. It simulated too slowly to verify overall functionality, but the ring oscillator and pad do work. The superscan cell consisting of one pin driver and associated memory also simulated successfully, as shown on the next page.

No floating wells were detected. The floating well check produced three nodes: Vdd, Vext, and Gnd.

Electrical characterization of the analog components was also performed, as described in the next section.

< insert superscan spice results here >

Electrical Characterization

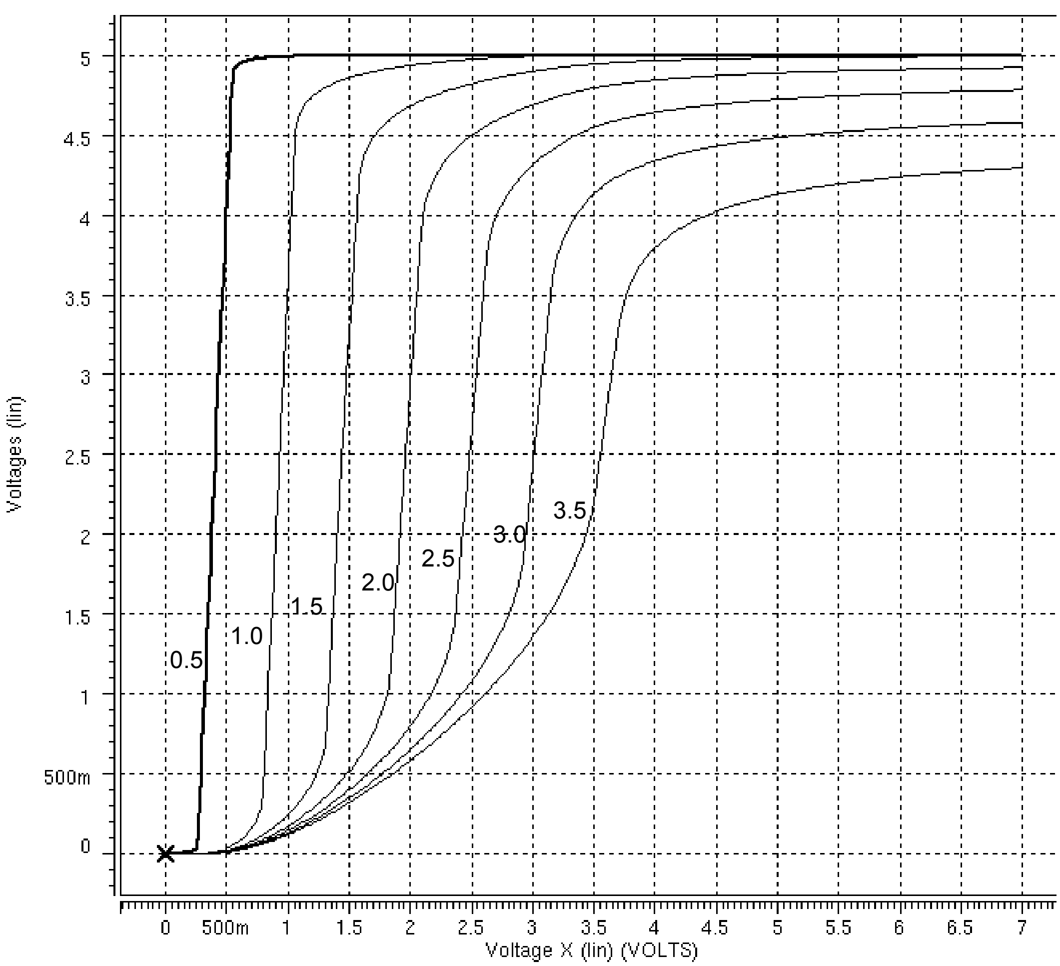
We characterized three circuits with HSPICE: the ring oscillator frequency, the input converter DC voltage transfer function, and the output converter I-V characteristics when connected in series with an output pad.

Ring Oscillator

The ring oscillator oscillates at approximately 125 MHz in SPICE. It is unlikely to swing rail-to-rail when driving a pad connected to a capacitive load; however, some oscillation should still be observable.

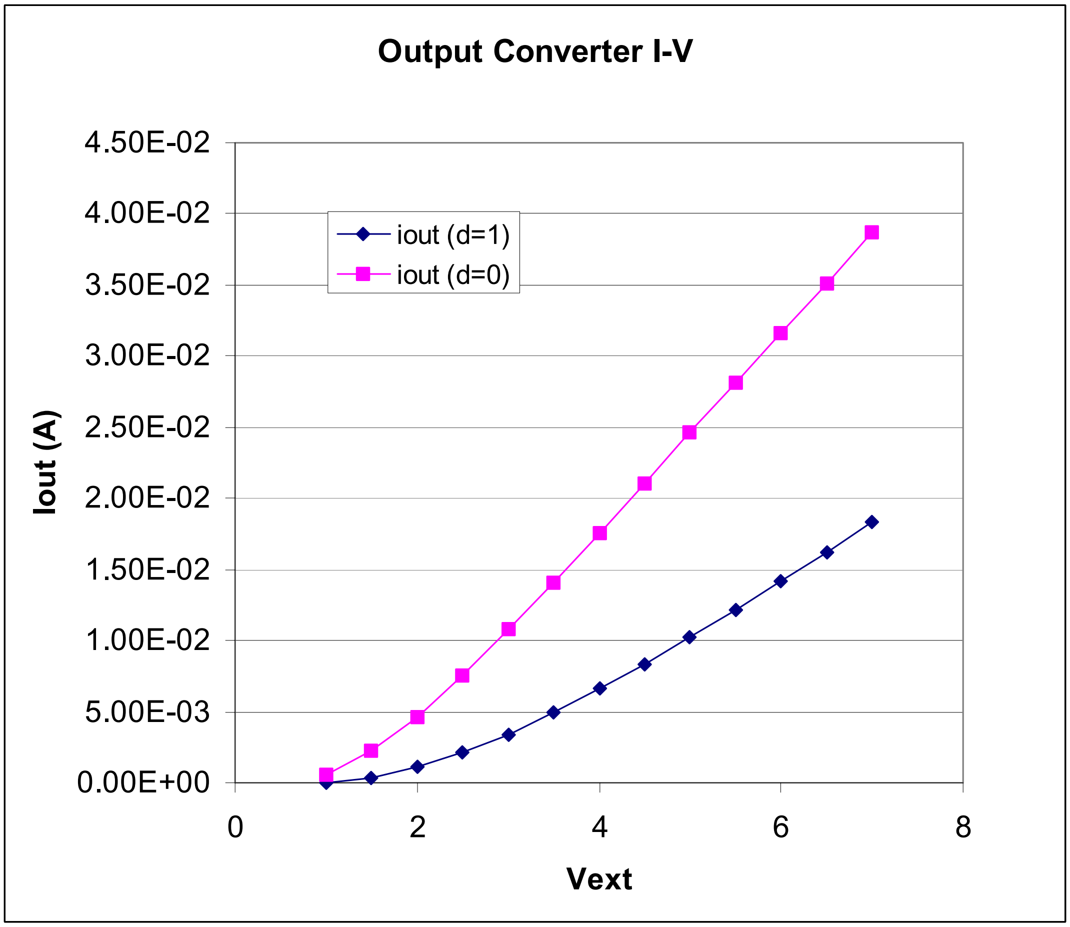
Input Converter

The input converter has the DC transfer characteristics shown below. The horizontal axis measures vin and the vertical axis measures vout. The different curves are labeled with different values of vextovertwo, the threshold voltage. The plot shows that the switching threshold is about vextovertwo, as expected. At higher threshold voltages, the output fails to pull all the way to Vdd. This is because the PMOS transistors in the current mirror are too weak relative to the NMOS input transistors. Nevertheless, the output is high enough to register as a valid input to the subsequent stage of logic, so the performance seems to be acceptable.

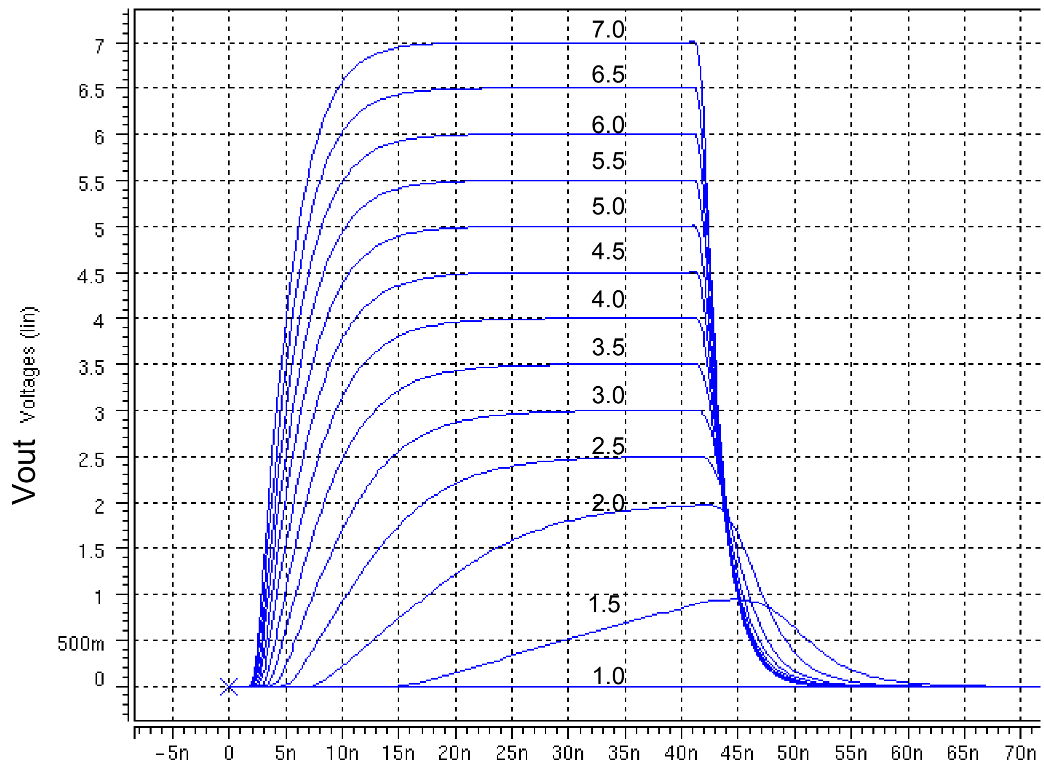


Output Converter

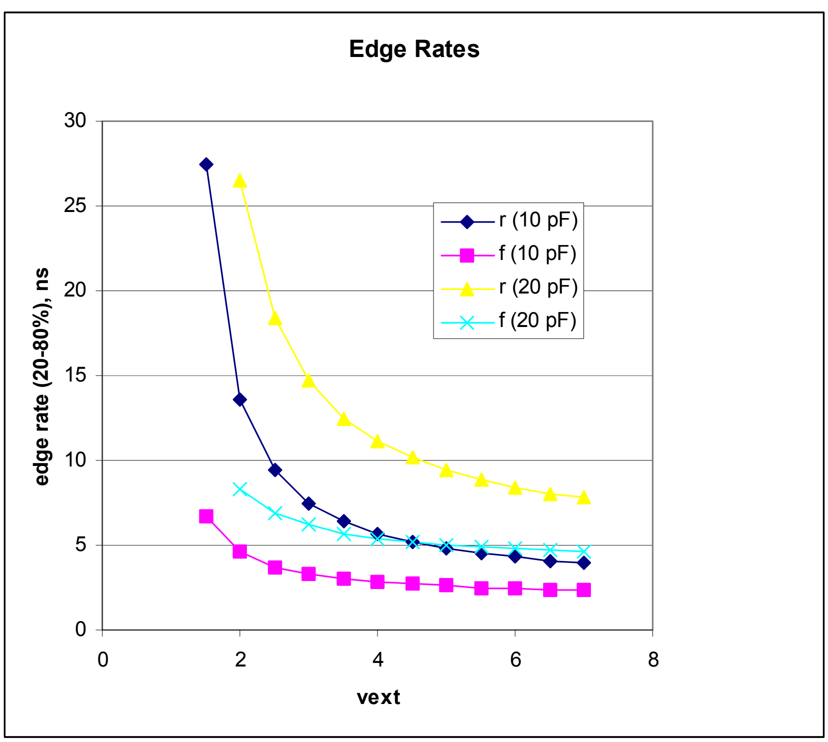
We characterized the output converter by measuring the output current vs. vext for high and low outputs shorted to low or high sources and by measuring the rise/fall of the output vs. vext driving 5, 10, and 20 pF loads.



The next figure plots the output pin voltage as a function of time driving a 10 pF load to various external voltages. The external voltages are labeled above each waveform. The rise time is greater than the fall time. The circuit fails to operate at all at an external voltage of 1.0; in this process, the threshold voltages are such that a minimum of 1.3 volts appears to be required.



The plot below indicates rising and falling edge rates into 10 and 20 pF loads. The edge rates are measured from the 20 to 80% points on the waveforms. These edge rates are longer than might be desired at the low end of the voltage range and are not well matched between rising and falling transitions.

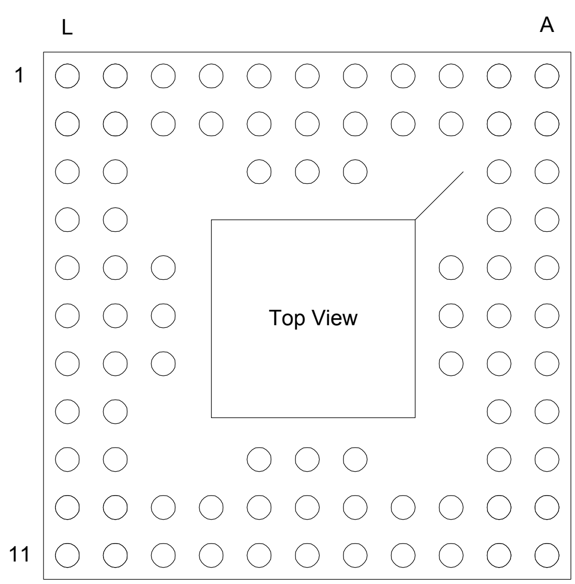


Pinout

The pin electronics chip has the following pinout, starting in the upper left corner of the chip going clockwise. (Be sure to check this; this pinout is from inspection and has not been verified).

Pin Name	Socket Pin
vext	K2
pin1	L1
pin0	J2
gnd	K1
vext	J1
vext	H2
gnd	H1
vdd	G3
ph1	G2
ph2	G1
sdin	F1
drive	F3
sample	E3
sdout	E1
vdd	E2
gnd	F2
vext	D1
vref	D2
gnd	C1
pin32	B1
pin33	C2
vext	B2
pin34	A1
pin35	B3
pin36	A2
pin37	A3
pin38	B4
pin39	A4
pin40	A6
pin41	B5
pin42	A5
pin43	C5
pin44	C6
pin45	B6
pin46	A7
pin47	B7
pin48	C7
pin49	A8
pin50	B8
pin51	A9
pin52	A10
pin53	B9
gnd	B10
pin54	A11
pin55	C10
pin56	B11
pin57	C11
pin58	D10
pin59	D11
pin60	F11
pin61	E10
pin62	E11
pin63	E9
pin31	F9
pin30	F10
pin29	G11
pin28	G10
pin27	G9
pin26	H11
pin25	H10
pin24	J11
pin23	K11
pin22	J10
gnd	K10
pin21	L11
pin20	K9
pin19	L10
pin18	L9
pin17	K8
pin16	L8
pin15	J7
pin14	K7
pin13	L7
pin12	L6
pin11	J6
pin10	J5
pin9	L5
pin8	K5
pin7	K6
pin6	L4
pin5	K4
pin4	L3
pin3	L2
pin2	K3

The figure below from MOSIS shows the pin labeling of the 84 pin PGA. For example, A1 is the pin in the upper right corner.



The pins are from the standard MOSIS pad frame. The vextovertwo (aka vref) and DUT pins use a special I/O pad called ESDONLY connected to Vext instead of Vdd. The pad has the standard MOSIS ESD protection circuits including thick oxide transistors and diode clamps. The pad is connected to the internal circuitry through a ndiff resistor 37 microns long and 16 microns wide with an expected resistance in the range of 100-150 Ω.

Test Results

All parts were operational. They are being used in the TestosterICs chip tester produced by One Hot Logic (www.onehotlogic.com). Measured data from two of the chips indicates:

Voltage range-
chip 1: 1.23 V - 6.5+ V
chip 2: 1.21 V - 6.5+ V

Edge rates-

chip 1:

	rise	fall
6 V	24 ns	19 ns
5 V	24 ns	19 ns
3.3 V	31 ns	22 ns
2.5 V	41 ns	24 ns
1.8 V	66 ns	31 ns
1.25 V	184 ns	48 ns

chip 2:

	rise	fall
6 V	24 ns	18 ns
5 V	26 ns	20 ns
3.3 V	33 ns	23 ns
2.5 V	41 ns	25 ns
1.8 V	68 ns	30 ns
1.25 V	183 ns	47 ns

Current-

chip 1:

	high	low
6 V	14.56 mA	22.04 mA
5 V	10.99 mA	17.66 mA
3.3 V	5.22 mA	10.12 mA
2.5 V	2.81 mA	6.45 mA
1.8 V	1.14 mA	3.21 mA
1.25 V	0.27 mA	1.15 mA

chip 2:

	high	low
6 V	14.42 mA	21.96 mA
5 V	10.88 mA	17.59 mA
3.3 V	5.12 mA	10.03 mA
2.5 V	2.80 mA	6.35 mA
1.8 V	1.14 mA	3.17 mA
1.25 V	0.25 mA	1.14 mA

Schematics

The pages in this section contain schematics of the following cells:

Cell	Purpose
core	The top level cell, including pads (a misnomer)
scan16	sixteen tiled superscan cells
superscan	scan cell with input and output converter
oc	output converter
andorshift	CVSL AND/OR gate level shifting to Vext
outbuf	large output driver powered by Vext
invext	inverter powered by Vext
icscancell	scan cell with input converter
ic	differential amplifier input converter
scancell	scan chain for one DUT pin
mux	2-input multiplexer
tristate	inverting tristate driver
inv	inverter
latch	static latch
ring	ring oscillator enabled when sample is high
inv8	8x inverter
pads84	pad frame
inpad	input pad
outpad	output pad
esdonly	unbuffered pad with ESD protection using Vext

(not available in this version)

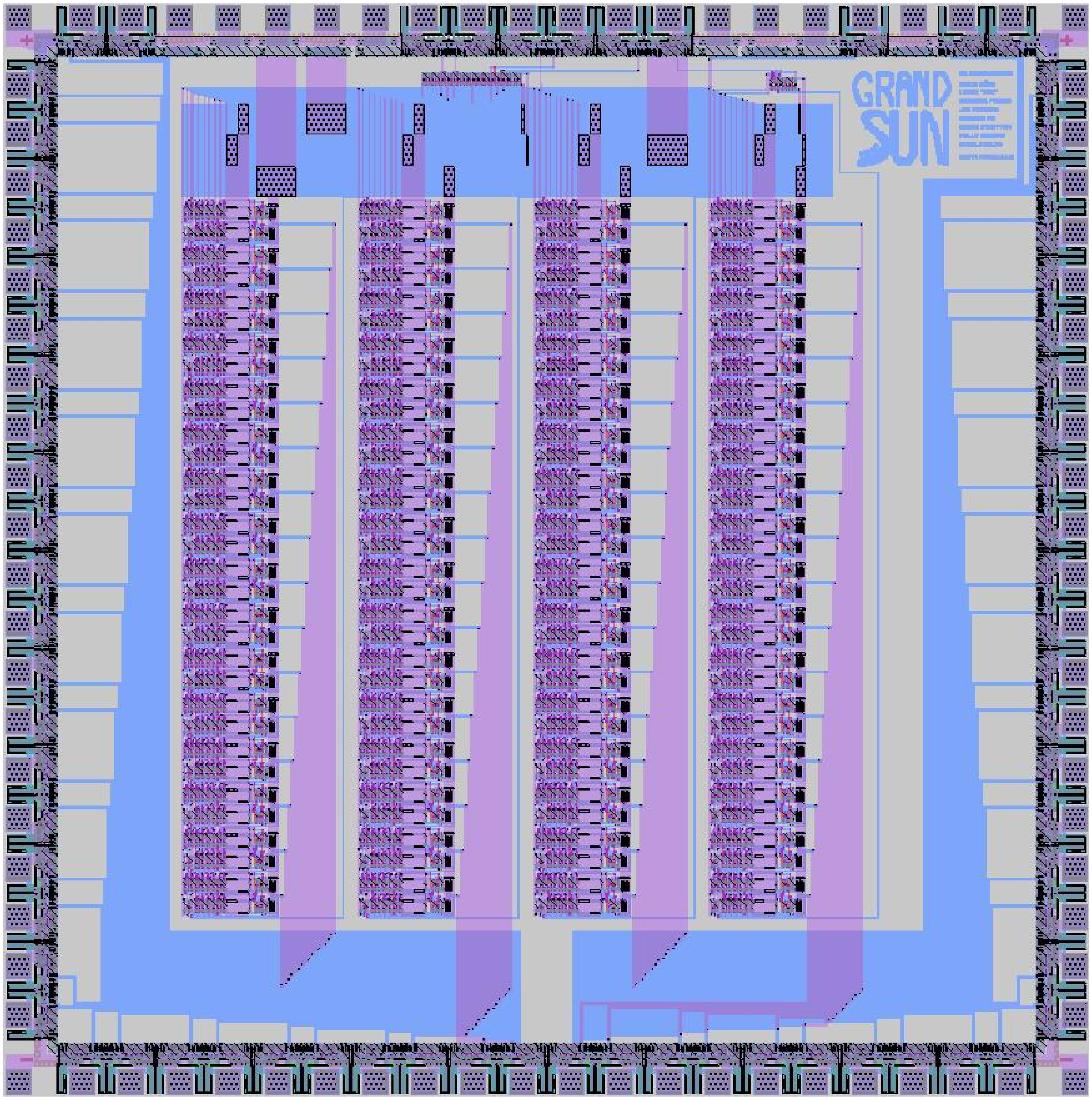
Layout

The pages in this section contain layout of the following cells:

core (color plot)
core
scan16
superscan
oc
andorshift
outbuf
invext
icscancell
ic
scancell
mux
tristate
inv
latch
ring
inv8
pads84
inpad
outpad
esdonly
gnd
vext
vddleft
vddright
cg
cg_r
cv
cv_r

(not available in this version)

core



Appendices

Appendix I: Specifications for custom chip for GrandSun of MacTester

By Stephani Ordinario, Sun Clinic Team

Performance

- Edge rates < 5-10ns into a 20pF load
- 5mA<Output current <10mA
- Operates at Vdd (5V)
- ESD tied to Vext supply, I/O pins ESD protected to survive Machine/Human Body Model
- 84-pin package
- Drives 64 I/O pins

Inputs

- ph1
- ph2
- ph1 and ph2 are non-overlapping clocks
- Vdd (3 pins – 2 pads, 1 logic)
- Vext (1-7V) (5 pins)
- Vref (1 pins)
- GND (5 pins)
- Sdin – even bits are enable, odd bit are dout for each I/O pin
- Drive
- Sample

Outputs

- 64 I/O pins
- Sdout

Input Control

Data is transmitted in serial to sdin. When drive is low, at each rising edge of ph2, one bit from sdin is loaded into latches in a scan chain until sdin is fully stored. Data is held until drive is asserted, when all 64 data values are converted (Vdd to Vext) then applied, simultaneously to 64 I/O pins.

Output Control

When sample is asserted, data is copied from 64 I/O pins in parallel, converted back (Vext to Vdd), and latched. At each rising edge of ph1, when sample is low, data bits travel back through the scan chain and out to sdout.

Additional Recommendations

- 1.2 or 2.0 micron process
- 4.60 x 4.70mm die size
- osc (output of a ring oscillator) for internal testing purposes

Appendix II: Tapeout Procedure

Harvey Mudd Guide to Fabricating Chips through MOSIS

David Harris

11/14/99

Read all of these steps a month before planning to send out your chip. The accounting has a significant lead-time.

Design your chip

Generate .cif from Magic
magic –T scmos2 (see notes below)
:cif ostyle lambda=0.8(nwell)
:cif write core
look at CIF file, make sure it has no CWP pwell layer

Read cif back in to check
copy cif to another directory
:cif istyle lambda=0.8(nwell)
:cif read core
-- *drc*
:drc why   No errors should be detected (see notes below)
-- *functionality*
:ext style lambda=0.8(scna16_ami)
:extract
ext2sim core.ext
irsim scmos50.prm core.sim, make sure function is correct
-- *layout vs. schematic check*
gemini core.ext coresue.ext
-- *SPICE simulation (if applicable)*
ext2spice core.ext
look for floating capacitors in core.spice. Remove if necessary with rmfloat.pl core.spice
hspice core.hsp
-- *floating well check*
:extract style check_nwell
:extract all
ext2sim core.ext
irsim scmos50.prm core.sim, see notes below
--*well routing check*
magic –T scmosWR
:cif istyle lambda=0.8(nwell)
:cif read core
:extract all
ext2sim core.ext
irsim scmos50.prm core.ext, see notes below
-- *floating well and well route scripts*
see notes below
-- *generate checksum*
cksum core.cif, see notes below

To plot a magic file in black and white:
:cif ostyle plot
:cif write core
pplot –k core.ps core.cif

Be sure MOSIS account has money in it
Often this requires sending a PO two or three weeks in advance.

Send new project and fabricate request
Use the MOSIS web form to create a new project with the following information (adjust the fields for your process, package, and pin count).
REQUEST: NEW-PROJECT
CUSTOMER-ACCOUNT-NUMBER: 2170-COM-UNIV/HMC-E
CUSTOMER-ACCOUNT-PASSWORD: CSNLVRY (or maybe PREREIRAD)
DESIGN-NAME: GRANDSUN2 (change this)
DESIGN-PASSWORD: OFMACTESTER (change this)
PHONE-NUMBER: (909) 607-3623
DESCRIPTION: Pin electronics for chip tester
TECHNOLOGY-CODE: SCN
LAMBDA: 0.8
DESIGN-SIZE: 4420 X 4450
PADS-COUNT: 84
NET-ADDRESS: David_Harris@hmc.edu
PO-NUMBER: B0002522
QUANTITY-ORDERED: 15
PACKAGE-NAME: PGA84M
REQUEST: END

When you get a new project approval, send the following fabricate email to mosis@mosis.org
REQUEST: FABRICATE
DESIGN-NUMBER: 59316 (change this to what was returned by newproject request)
DESIGN-PASSWORD: ofmactester
LAYOUT-CHECKSUM: 13598746,281090
LAYOUT-FORMAT: CIF
LAYOUT:
(paste CIF file here)
REQUEST: END

Expect confirmation from MOSIS consisting of:
NEW-PROJECT accepted
FABRICATE accepted
    be sure account is billed for Discount, not Standard rate
DESIGN CHECK accepted
Design being fabricated
Design being shipped (about 3 months later)

Notes:

(1) At the moment, the default Stanford scmos technology file lacks the setup to CIF out in the lambda=0.8(nwell) style. For the GrandSun2 of Mactester submitted 11/15/99, we created a new scmos2.tech27 technology file in which the cif ostyle lambda=0.8(gen) style was renamed lambda=0.8(nwell) and the PWELL generation was deleted. In the long term, a better technology file with more cif out styles should be prepared.

(2) The 0.8-micron io pads supplied by MOSIS have a 3-lambda spacing from diffusion in the input protection resistor. This leads to a DRC error. This is tolerable.

(3) For floating well check, watch for the feedback from irsim. If it reports that your layout has only two nodes, e.g.: *** IRSIM version 9.3 *** 2 nodes; transistors: parallel txtors:none then you don't have floating wells. If you have more than two nodes you may have floating wells. You can get an idea about where the floating wells are by using the command ? * This will show you all the nodes in the circuit. All nodes except Vdd and Gnd are floating well nodes and their hierarchical name shows in which cell they are located. For people that are using padroute: It is possible that you will get 3 nodes in that test. Make sure that your third node corresponds to the Gnd of the pad ring. (that is because the padroute frame uses different Vdd and Gnd for the pad xtors and thus the wells of the pad xtors will be connected to something else than Vdd or Gnd).

(4) If you had routed power through a well, your simulation should not work and probably you will get complaints about parallel transistors. If your test cases run you are set.

(5) cksum is a program provided by MOSIS that generates a checksum and length of the file, ignoring characters like carriage returns and linefeeds that may be munged during file transfers. If it is not installed on the local machine, it can be downloaded and compiled from MOSIS.

(6) consider adding the floating well and well route scripts from EE272 at Stanford later.

Appendix III: Original GrandSun Test Chip Documentation

Note: This chip was fabricated and tested at Sun. It was fully functional except that the enable and dataout values are inverted relative to the inputs; this can be compensated for in software. The chip also lacked ESD protection and several were damaged during testing.

GrandSun of MacTester

David Harris
4/24/99

Introduction

The Harvey Mudd / Sun Microsystems 1999 Clinic project involved the design of a variable-voltage tester. The tester is enormous, at about 18 square inches. The incremental cost of each pin is also very high because of the low integration levels of the input and output converters. This tester has been known as the Son of MacTester, the MacTester of Sun, or the Sun of MacTester.

This document describes a proposed new tester using the same interface as the Sun Microsystems tester but constructing the pin electronics from custom MOSIS chips. A prototype was constructed using the Tanner Tools at Harvey Mudd College. The new tester will be called the GrandSun of MacTester.

Architecture

The GrandSun of MacTester follows the same architecture as Sun of MacTester, save that the pin electronics, consisting of data storage and level shifting that was formerly done by slave FPGAs, CMOS switches, and quad comparators, is now done by dedicated chips. This architecture is shown in Figure 1:

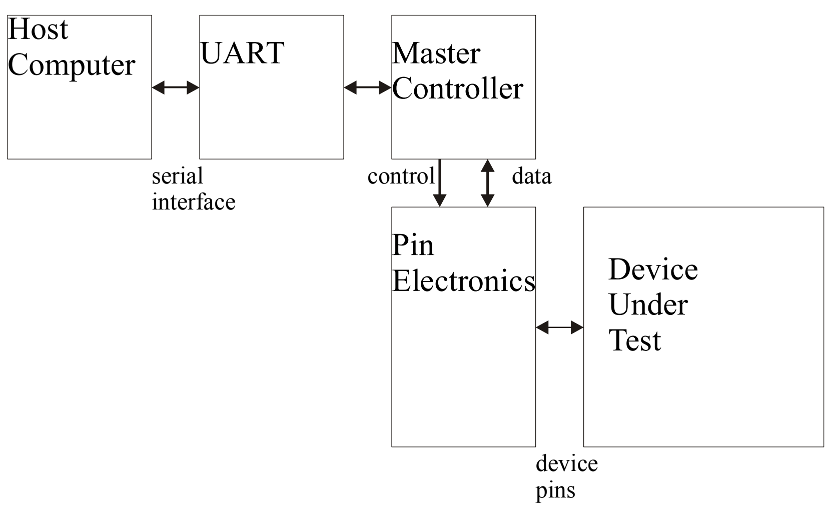


Figure 1: GrandSun of MacTester Architecture

The new architecture greatly reduces size and manufacturing complexity and potentially reduces cost by replacing the slave FPGA and dozens of quad package CMOS switches and comparators with a single custom pin electronics chip. The pin electronics chip has the interface shown in Figure 2. It uses two-phase non-overlapping clocks ph1 and ph2 to shift data in from sdin and out to sdout through a scan chain. When drive is asserted, the data is applied to the DUT pins. When sample is asserted, the data is read from the pins back into the scan chain. There is one pin logic block for each DUT pin handled by the tester. In addition to the control and data, supplies are required to handle the level shifting and comparison. These include GND, the standard 5 volt VDD for the digital logic, Vext, the external supply voltage used to operate the DUT, and Vref, the threshold between high and low. Vref is commonly set to Vext/2. The remainder of the chips in the package may be dedicated to I/O pins driving the DUT.

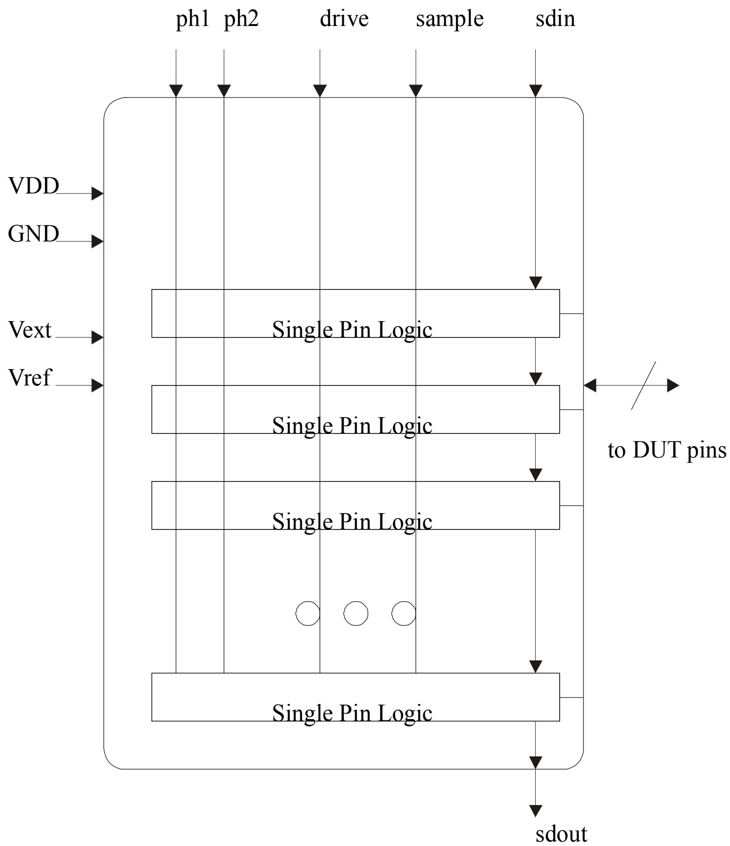
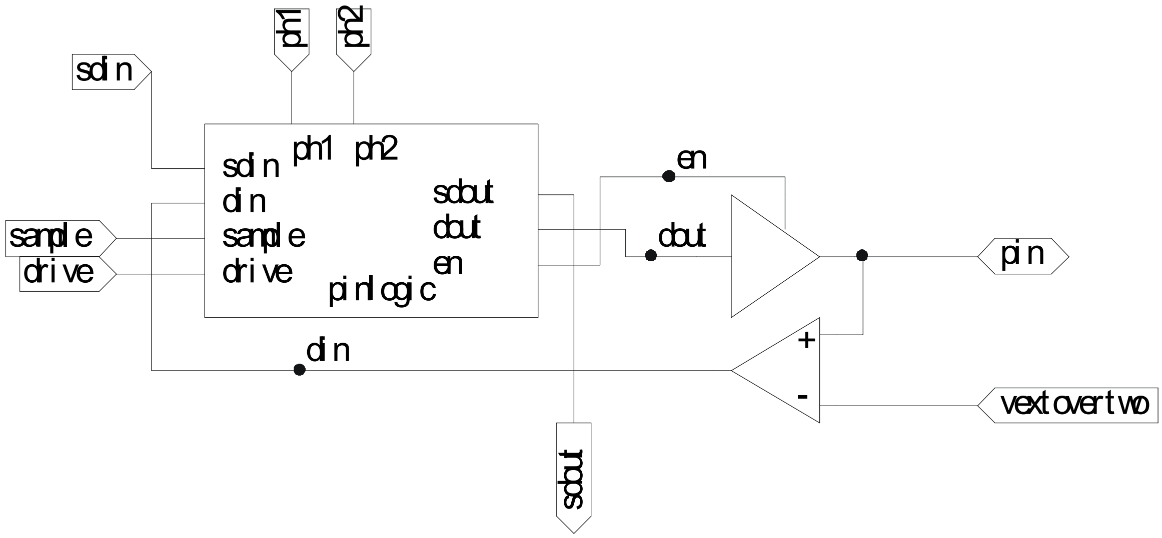


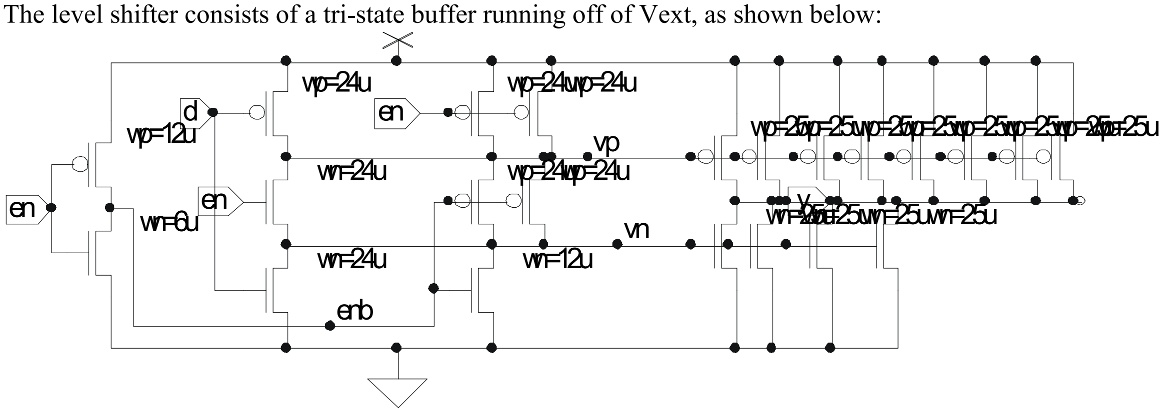
Figure 2: Pin Electronics Chip

Pin Logic

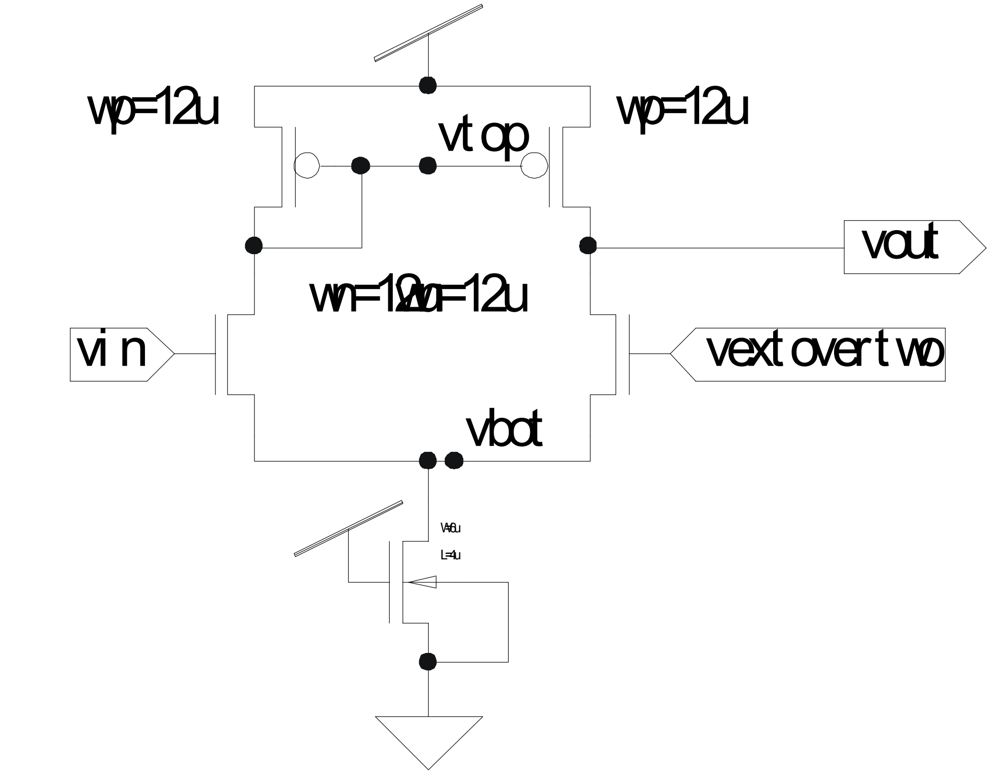
An individual block of logic controls each pin. The logic must be able to drive the pin high, low, or tri-state. Therefore, two bits of control are required. These two bits are shifted through a scan chain that links all of the pin logic blocks. Additional latches are required to hold the values driving the DUT so that the DUT inputs do not change while the scan chain shifts. A level shifter built from two inverters adjusts the 5-volt logic level used internally to a 1-7 volt Vext level driving the DUT pins. A comparator receives outputs from the DUT and translates the results back to 5-volt levels. Finally, these results can be inserted back into the scan chain. The pin logic block is shown below:



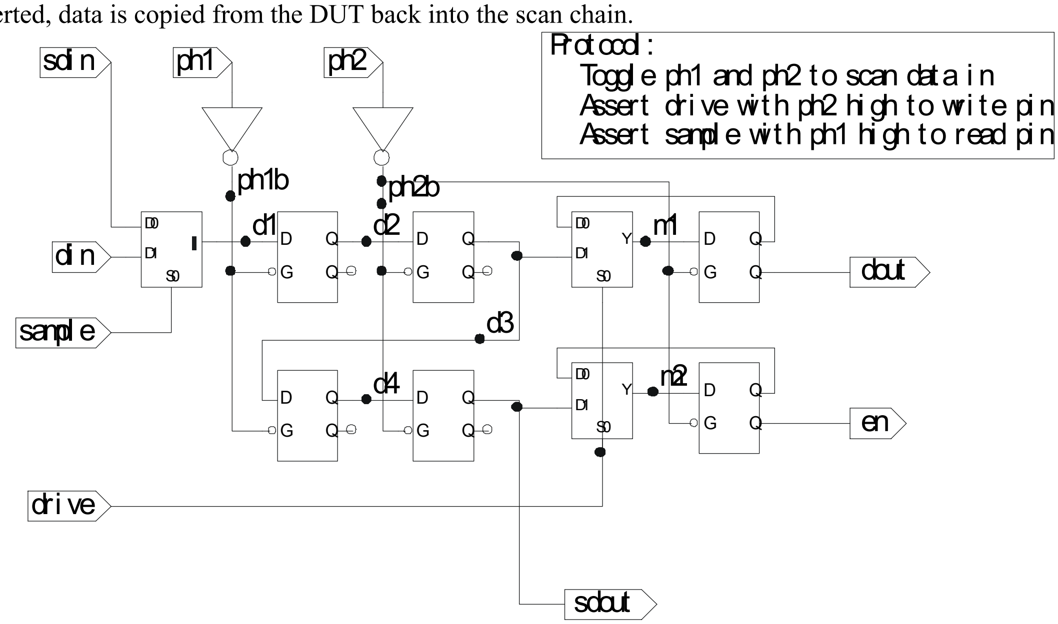
The level shifter consists of a tri-state buffer running off of Vext, as shown below:



The comparator is a simple differential amplifier:



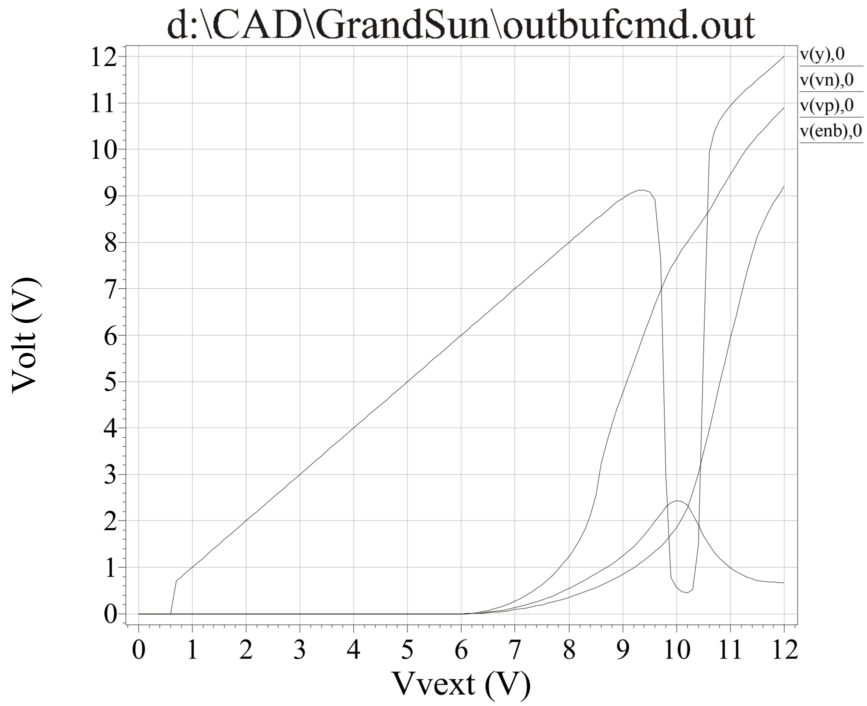
The scan chain and control logic are shown below. Data is marched through the scan chain by toggling non-overlapping clocks ph1 and ph2. When ph2 is high and drive is asserted, data is copied from the scan chain into the drive latches that control the value driven to the pin. When ph1 is high and sample is asserted, data is copied from the DUT back into the scan chain.



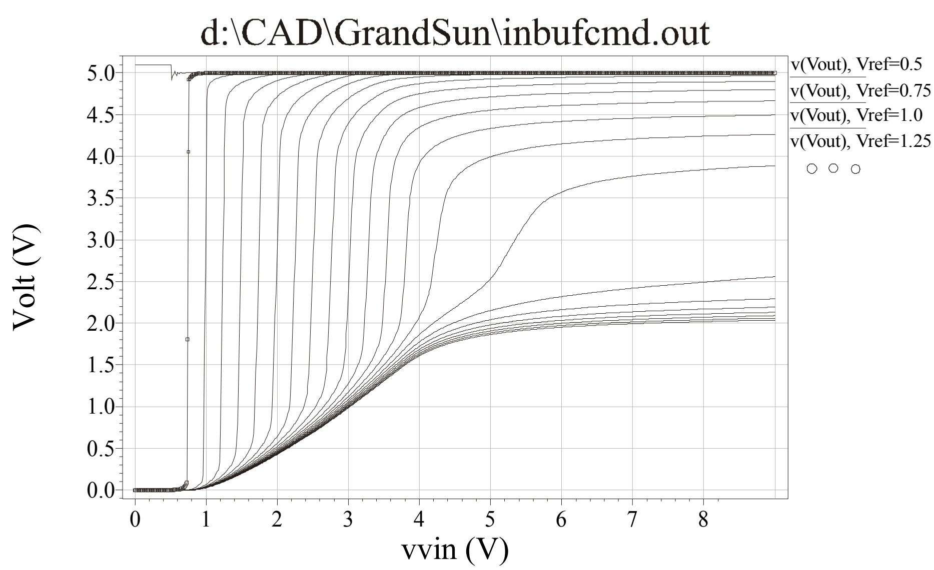
Verification Results

A MOSIS TinyChip has been designed to verify the GrandSun of MacTester. On account of space limitations, only 8 pin drivers are included; with some effort many more should fit on a TinyChip and plenty should fit on a 1.2-micron chip. The design used the Tanner Tools for schematic entry, T-Spice simulation, layout, DRC, and LVS. The comparator and level shifter were simulated in T-Spice for proper operation and LVS was used to match the layout against the schematics. The design is DRC-clean in LEdit, though the CIF does not pass DRC when imported into Magic. This appears to be caused by artifacts of Magic's DRC rules applied to standard cells and to the pads.

The figure below shows the level shifter output voltage as a function of external voltage, assuming VDD=5v. The level shifter does not operate below a threshold voltage (about 0.7v). It also fails above 9.5 volts, as indicated by the deep trough in the otherwise straight line. It appears that the level shifter is fully operational between 1 and 7 volts.



The next figure shows the comparator output voltage as a function of the input voltage for various reference voltages. With a reference voltage of 0.5 volts, the comparator fails because the reference is outside the common mode voltage range of the comparator. The remaining curves are on 0.25 volt spacings of reference voltages, so the comparator works well with references in the range of 0.75-4 volts, after which it again performs poorly. If Vref is set as Vext/2, the comparator limits the tester to inputs between 1.5 and 8 volts, missing the target minimum 1 volt Vext. The tester may still work with Vext = 1 and Vref = 0.75, but the noise margins will be degraded.



Pin Interface

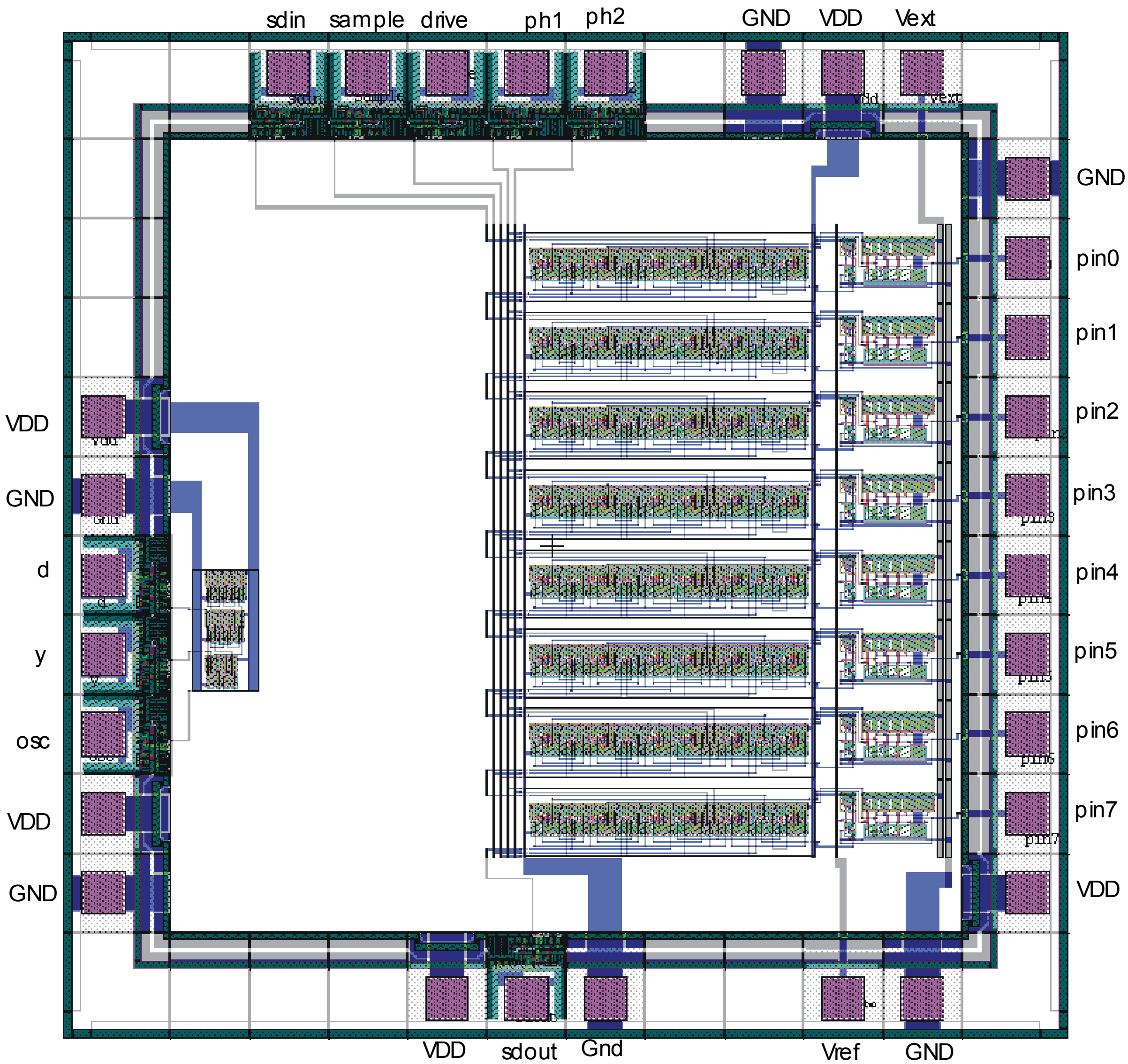
The chip tester uses the following pin interface (assuming the same bonding as a standard tiny chip):

Pin	Direction	Function
1	IO	pin3
2	IO	pin2
3	IO	pin1
4	IO	pin0
5		GND
6		Vext
7		VDD
8		GND
10	in	ph2
11	in	ph1
12	in	drive
13	in	sample
14	in	sdin
19		VDD
20		GND
21	in	d
22	out	y
23	out	osc
24		VDD
25		GND
29		VDD
30	out	sdout
31		GND
34		Vref/2
35		GND
36		VDD
37	IO	pin7
38	IO	pin6
39	IO	pin5
40	IO	pin4

The d, y, and osc pins are used for chip functionality test circuits. d is connected to y through two pads and an inverter. osc is the output of a 9(?) stage ring oscillator driven out through a pad.

Note that the IO pins and VDD, GND, Vext, and Vref/2 pins have no ESD protection. The standard guard rings operate at GND and VDD, causing potential problems on the I/O pins and Vext if the voltages exceeded VDD (5 volts).

A chip plot is shown below, annotated with pad names.



Future Directions

The prototype design lacks several features needed for a complete design. The area of the pin logic should be compacted to drive at least 28 pins in a TinyChip 40-pin package. Using larger packages and better processes should allow far more pins and utilization of a higher fraction of the pins.

The present design has no ESD protection on any of the I/O pins because the standard ESD connects to a 5 volt supply rather than Vext, leading to forward biased diodes when a 7 volt Vext is used. A better design would include ESD structures tied to the Vext supply. Also, more attention should be paid to edge rates and current drive capability.

The operating range of the tester would be greater if the common mode range of the comparator could be increased. A better comparator design handling low voltages would be useful.

The present design also relies on an external UART and master FPGA. In a better process with a pad-limited die, the UART and master controller could be integrated onto the pin electronics chip. A single mode pin could configure a pin electronics chip as a master or slave. The master would devote several pins that normally drive the DUT to instead provide the UART interface and would contain an FSM that drives the control signals and scan chain between daisy-chained pin electronics chips. This would result in a system containing only a clock oscillator, a serial transceiver, the DUT socket, and pin electronics chips, along with miscellaneous hardware such as the power-on LED and reverse voltage protection.

Notes on the LEdit CAD tools:

The morbit2n design rules now include overlaps of 1.5 lambda around contacts to diffusion or polysilicon. Old MOSIS rules used only 1 lambda and produced much cleaner layouts and needed no half-lambda dimensions. The new rules are in http://www.mosis.org/New/Technical/Designrules/scmos/scmos-contact.html. It would be nice to go back to the old rules or at least understand the motivation for the new rules.

The extract definition file is in: C:\TannerLb\LEdit\TECH\mosis\morbn20.ext
These files are compatible with the standard cell library and pads. They must go with the .tdb setup files also in TannerLb. The setup and extract definition file in
C:\Program Files\Tanner EDA\L-Edit 7.50\tech\mosis\morbn20.ext
are newer and incompatible with the library.

The standard cell library is inconsistent on the direction of use of metal1 and metal2. In particular, M1 is used horizontally for power lines, yet also vertically on the side of the cells for power tieoffs.

LEdit is incompatible with my ATI video card. It hangs fairly often, requiring a hard reset. The problem was fixed by installing a beta version of a new ATI video driver.

Before running LVS, make the following changes to the .sp file from the schematics:
.include models.md
.param l=1u
replace Subs with Gnd in main cell

Guidelines to interpreting LVS errors:

1) devices match in number, but nodes don't match.
    caused by bad latch schematic in scmos library. Fixed Gb to G2 and it matches
2) problems from parallel legs: turn on "optimize network"
3) .sp file has connections to Subs node (substrate)
    why should this be? Workaround: change subs to Gnd in top level .sp file
4) mismatch in size on pads
    error in schematics: wrong size on pad transistor in cell library. LVS without pads for size, then do a complete LVS ignoring size errors. LVS does not sum widths of parallel transistors when doing "optimize network."

I frequently get an undo buffer error in Sedit, but it seems to cause no problems.

Tspice doesn't converge on uninitialized latch nodes. This is a problem for simulating layout because hierarchy is lost, making identification of latches very hard.

References

Harvey Mudd College Sun Clinic Project Report, A. Barber, J. Gainsley, F. Shaw, L. Joe, and R. Willingham, 1999.