

Lab 1: Electrical Characteristics of Logic Gates SOLUTIONS

Digital Design and Computer Architecture: RISC-V Edition (Harris & Harris, Elsevier © 2021)

Grading Rubric: See points in brackets below. Half credit for wrong but thoughtful answers.

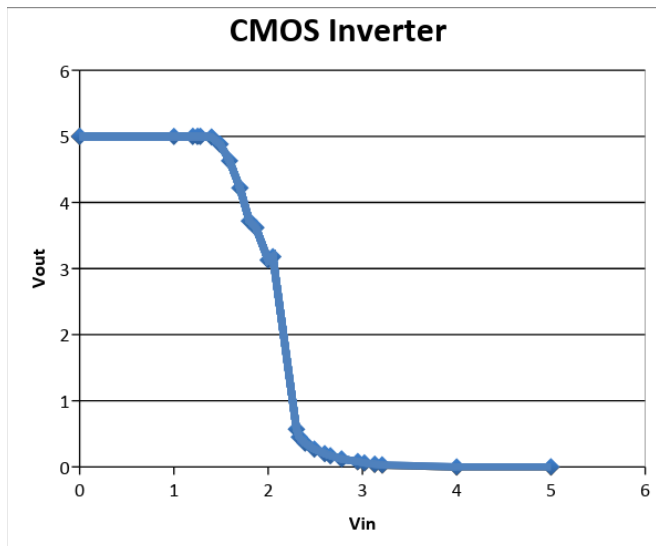
Please indicate how many hours you spent on this lab. This will be helpful for calibrating the workload for next time the course is taught.

1. Gates, Switches, and LEDs

- a) [1] What resistor values did you choose? Why? $R1 = 10\text{ k}\Omega$ to keep current reasonably low but not cause a significant drop due to inverter input current. $R2, R3 = 330$ or 270 ohms to get about 10 mA of LED current. In general, $R1$ of $0.5\text{--}100\text{ k}\Omega$ would all work tolerably, and $R2/3$ of $150\text{--}500\text{ ohms}$ would be fine.
- b) [1] Did your circuit function correctly? YES

2. Transistor-level Inverter

- a) [2] Plot of VTC



- b) [1] Input and output logic levels:

$V_{IL} = 1.5$, $V_{IH} = 2.3$, $V_{OH} = 4.88$, $V_{OL} = 0.45$

(these may vary slightly for your circuit depending on the balance between the pMOS and nMOS transistors.)

- c) [1] High and low noise margins:

$NMH = V_{OH} - V_{IH} = 2.58$, $NML = V_{IL} - V_{OL} = 1.05$ (these may vary slightly based on the input and output logic levels from part b)

3. Ring oscillator

- a) [2] Oscilloscope trace of switching output, annotated with the period and frequency. 30.7 MHz , 32.5 ns typical. This will vary a bit with the chip and wiring.

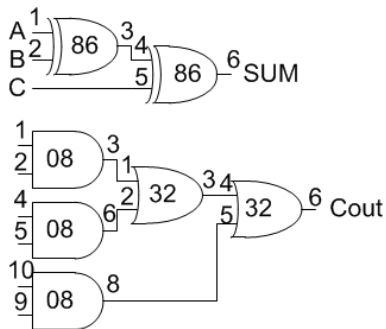
- b) [1] Compute the average delay of a single inverter from the ring. With five stages and both a rise and fall event per stage, the delay per inverter is $(32.5 \text{ ns}) / (5 * 2) = 3.25 \text{ ns}$. This compares to 7 ns in the NXP datasheet at 5V, 15 pF, and is lower because the capacitance is lower.
- c) [1] Why does the frequency change when you touch the wires? I observed the frequency drop from 30.7 to 30.3 MHz when I touch the wires because of the extra capacitance of my body.
- d) [2] Measured power consumption for both the ring oscillator and the powered quiescent chip 18 mA (may vary modestly depending on the chip and your wiring) for the ring oscillator. Current is less than 0.2 μA , the bottom of the scale of the meter, for the quiescent chip. Convert to power by multiplying by voltage (5V): 90 mW ring oscillator / 1 mW quiescent.

4. Full adder

- a) [1] Truth table

Inputs			Outputs	
C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

- b) [2] Schematic



- c) [1] Do your measured outputs match your truth table in all eight cases? YES