Digital Design and Computer Architecture

Labs Overview

Introduction

These labs accompany the textbook *Digital Design and Computer Architecture, 2nd Edition, Harris & Harris, Elsevier, 2012*. The labs show you how to design and implement digital circuits using Altera's Quartus II software and DE2 FPGA board. The Quartus II software is a powerful and popular commercial suite of applications used by hardware designers. Below is a list of the labs.

Lab 1	Full Adder
Lab 2	7-Segment Display
Lab 3	FSM: Adventure Game
Lab 4	FSM: Thunderbird Turn Signal
Lab 5	ALU
Lab 6	C Programming
Lab 7	Temperature Control
Lab 8	MIPS Assembly Programming
Lab 9	MIPS Single-Cycle Processor
Lab 10	MIPS Multicycle Processor (Part I)
Lab 11	MIPS Multicycle Processor (Part II)

The labs begin with combinational and then sequential circuit design and work up to designing two MIPS processors. In Labs 1 and 2 you will design and build combinational circuits using schematic entry. Lab 3 uses schematic entry to design a finite state machine (FSM). In Labs 4-5 and 9-11 you will use SystemVerilog to enter your designs. Lab 4 is another FSM, but this time using SystemVerilog for design entry into Quartus II. Labs 6-7 are optional labs on C Programming. In Lab 8, you will write a MIPS assembly program to perform floating point addition. You may use QtSpim (instead of MPLab, as described in the lab) to simulate the MIPS assembly program. QtSpim, a MIPS simulator, is available for download here: http://spimsimulator.sourceforge.net/. In Lab 9, you are given the SystemVerilog code for the single-cycle MIPS processor described in the textbook. Then you modify the processor so that it performs two additional instructions. In Labs 10 and 11 you design the MIPS multicycle processor described in the textbook.

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