Errata

CMOS VLSI Design
4th Edition

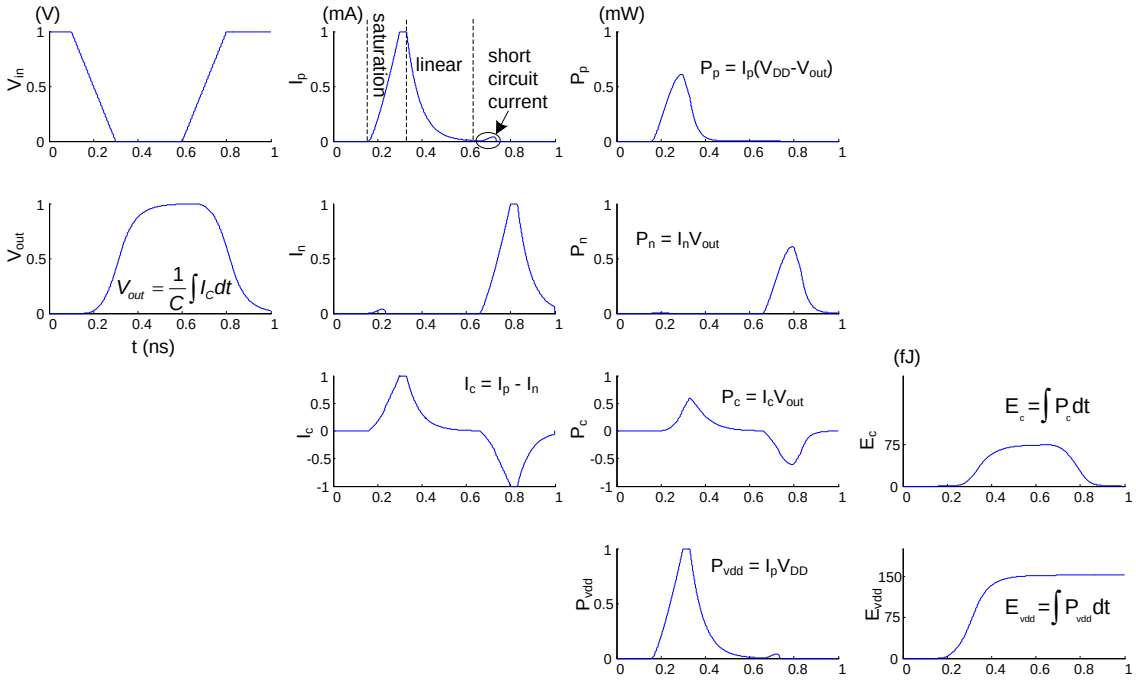
Last updated 5 December 2011
Send your corrections to bugs@cmosvlsi.com

p. 188, Figure 5.12: The activity factors fail to take into account the fact that the internal nodes are not statistically independent. By writing out a truth table and considering each possible input, we can compute the corrected node probabilities to be $p_4 = 1/8$, $p_5 = 7/8$ and activity factors $\alpha_4 = \alpha_5 = 7/64$. These revised activity factors should be used in EQ (5.17). (J. Frenzel 9/28/11)
p. 511, 4th sentence of paragraph under Example: "to drive a global **wordline**" -> "to drive a global **bitline**." (J. Frenzel 12/5/2011)

The following corrections have been made in the 2nd printing (Summer 2011):

p. 67, EQ 2.9: add a superscript 2 after the close parenthesis V. Ramachandra 3/27/10
p. 67, EQ 2.11: A -> μA Yihuan Huang 9/25/10
p. 148, Example 4.2 Solution 1st paragraph: "Two pMOS" -> "Three pMOS" M. Kulkarni 1/8/11.
p. 152, "Figure 4.15(b) shows the equivalent circuit for the **falling**" -> "Figure 4.15(b) shows the equivalent circuit for the **rising**" (J. Ma, 5/22/10)

p. 183, EQ 5.8: "E_C" -> "E_{VDD}" DMH 2/16/10
p. 183: EQ 5.8: C -> C_L (K.T. Lau 5/6/10)
p. 183: Figure 5.5: The vertical scale on the energy plots was distorted. DMH 12/30/10



p. 195, EQ 520: switch N2 and N1 (DMH 12/30/10)

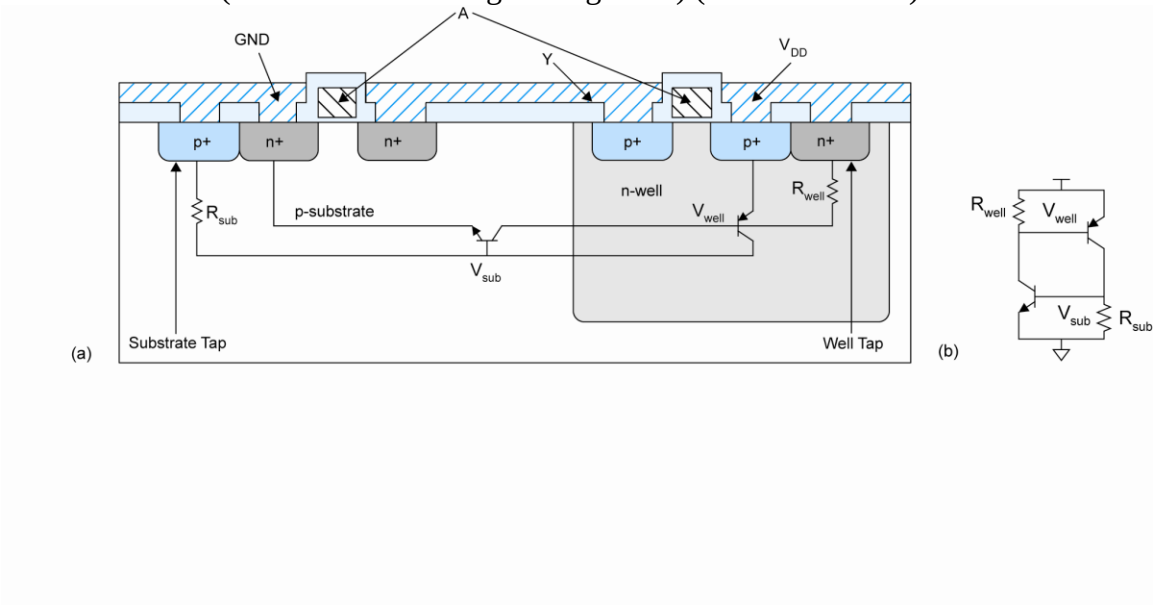
p. 196, Table 5.2 has some garbles. Corrected values are shown in bold (DMH 12/31/10)

Input State (ABC)	I_{sub}	I_{gate}	I_{total}
000	0.4	0	0.4
001	0.7	0	0.7
010	**0.7**	1.3	**2.0**
011	3.8	0	**3.8**
100	0.7	6.3	7.0
101	3.8	6.3	10.1
110	5.6	12.7	18.3
111	28.3	19.0	47.3

p. 209, problem 5.8: 4 FO4 -> 5 FO4 DMH

p. 237, EQ. 6.39: C_{wi+1} -> C_{wi} , close parenthesis damaged (J. Frenzel 10/26/11)

p. 253, Figure 7.12: the emitter of the npn transistor should connect to the nMOS source rather than drain (because the emitter goes to ground) (J. Nestor 2/4/11)



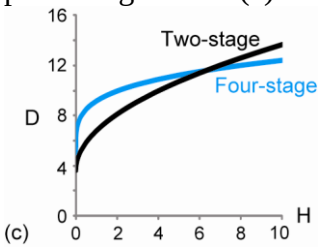
p. 273 example: "solve for Y_s" -> "solve for Y_c" DMH 12/26/10

p. 282, Figure 7.36 caption: Pentium III -> Pentium 4 (J. Dong 10/26/2011)

p. 292 last paragraph of 8.2.2: "source `Vgs`" -> "source `Vds`"

p. 346 Example 9.6: "H > 2.9" -> "H > 6.2" (T. Nguyen 2/1/11)

p. 347 Figure 9.43(c) should be (T. Nguyen 2/1/11)

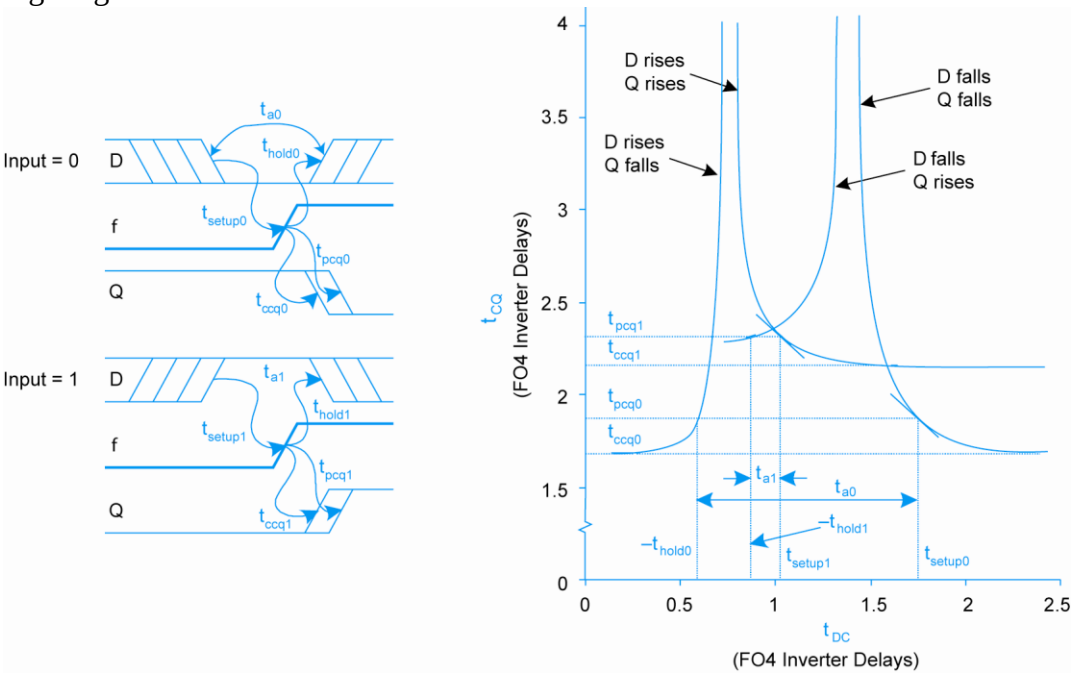


p. 351: line 1: swap V and Vbar (I. Tseng 12/20/10)

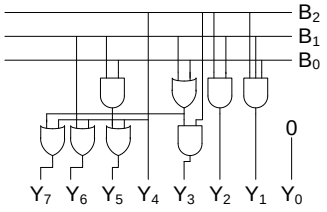
p. 406: (J. Frenzel 11/30/10) eliminate t_{ar}, t_{af}, define a new ta0 and ta1 as the time that the input must remain low or high, respectively to be correctly sampled at that value. Modify 10.20 to read:

$$t_{a0} = t_{setup0} + t_{hold0}$$
$$t_{a1} = t_{setup1} + t_{hold1}$$

Change Figure 10.36 to be:

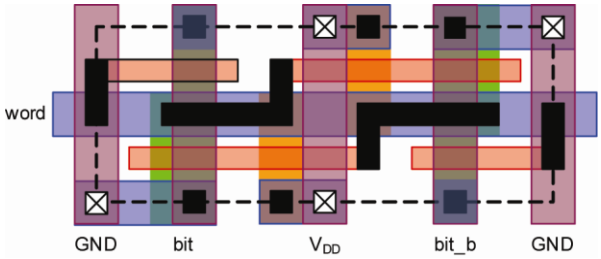


p. 462, Table 11.4: C -> Cbar in unsigned comparison of A > B DMH
p. 466: 11.5.4 Linerar -> 11.5.4 Linear
p. 473, Table 11.11: rows are in the wrong order. The shift type column should read: DMH
Rotate Right
Logical Right
Arithmetic Right
Rotate Left
Logical / Arithmetic Left
p. 474, Figure 11.66: $Z_{N-2:N}$ -> $Z_{2N-2:N}$ (V. Berrios 10/31/10)
p. 493, Figure 11.97(b): Y3 should be B2 * (B1 + B0) (S. Maurya 6/24/10)



(b)

p. 501, Figure 12.5, out_v1r -> out_b_v1r in label for waveforms (I. Tseung 12/20/2010)
p. 505, Figure 12.15 should be (D. Matthews 12/5/10)



p. 709, Table A.4: 161 -> 171 (V. Pedroni 3/2011)
p. 740, VHDL next to last paragraph: -2^{31} -> $-(2^{31}-1)$ (V. Pedroni 3/2011)
p. 831: phase-locked loops should be listed under PLLs rather than PPLs

Cosmetic corrections (DMH)
p. 187, 6th line: overbar on P is too far right DMH
p. 231: too much space between t and pd in many places
p. 237: right edge of 6.39 is cut off
p. 506, Figure 12.19: poly stipples broken in several places
p. 582, Figure 13.35: swap + and – terminals on op-amp (P. Jnanendra 2/26/2011)
p. 830: “See PPLs” -> “See PLLs” (J. Frenzel 4/20/2011)
p. 831: “PPLs” -> “PLLs” (J. Frenzel 4/20/2011)