High Speed CMOS Circuit Design

Syllabus

Instructors:

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Grading

The first half of this class will feature weekly assignments exercising the skills you learn in lecture and the readings. You are encouraged to discuss ideas with other engineers, but must turn in your own solutions, not a photocopy of a group solution. After the midterm, you will form 2-person teams for a major design project exploring high speed floating point multiplication. You will do most of your learning in this class while working on the assignments and project. Plan to spend many hours on the assignments, especially as the project kicks in.

- Problem Sets: 30% (your lowest problem set score will be dropped)
- Project: 30%
- Midterm: 30%
- Class Participation: 10%

Readings

- Weste & Eshraghian, *Principles of CMOS VLSI Design*, 2nd Edition, Addison-Wesley.
- Sutherland, Sproull, & Harris, *Logical Effort: Designing Fast CMOS Circuits*, El Cheapo Draft Publishing
- Selected key journal articles, handed out in class

Detailed Schedule:

Class meets from 6:30-9:30 Thursday evenings, with no class April 9. In general, the beginning of each class will be dedicated to discussion of the assignment due that day. There will also be hourly breaks to stretch or imbibe caffeine.

S1: 2/20: Logical Effort: Designing Fast CMOS Circuits

Logistics, SIA Roadmap, designing for speed on the back of an envelope, logical effort, tapered buffer chain sizing, effort-of-4 rule, examples, RC delay models, limitations of RC models: input slope, velocity saturation, fanout-of-4 (FO4) inverters, FO4 delay metric, optimal P/N ratio of inverters and other gates, alternate sizing methodologies

Readings:	Logical Effort Ch. 1-4, W&E Ch. 4.1-4.3.4, 4.5-4.6
Handouts:	Syllabus, SIA Roadmap, The Fanout-of-4 Inverter Delay Metric
Assignments:	Problem Set 1

S2: 2/27: Simulation & Static Circuit Families

simulation techniques, extracting parameters for back of the envelope calculation, curve-fitting gates to RC models, minimizing use of simulation, CMOS gate design: NAND/NOR issues, complex gates, skewed gates, logical effort revisited, early input optimization, asymmetric gates, stack height, tapered stacks & related fallacies; transmission gates: applications, P/N ratio, logical effort, series gate limits, NMOS-only vs. transmission gates, level restoration, noise margins, complementary pass transistor circuits, other pass transistor variants; pseudo-NMOS: review of NMOS, gate design, logical effort, drawbacks: noise margins, power consumption, ratio problems across process; solutions: IDDQ mode, current mirrors; symmetric NOR gates

Readings:	Logical Effort Ch. 5, 8-9, W&E Ch. 5.1-5.3 (skim), 5.4-5.4.3, 6.6
Handouts:	Low-power logic styles
Assignments:	Problem Set 2
Tools:	HSPICE

S3: 3/5: Dynamic Circuit Families & Circuit Pitfalls

Dynamic gate topology, skewing gates, series evaluation devices, advantages: speed, area, challenges: monotonicity, charge sharing, crosstalk, noise margin, subthreshold leakage; solutions: domino, dual-rail circuits (DCVS), self-timing, posponing nonmonotonic functions, intermediate precharge devices, shielding, keepers; logical effort, gain effects of dynamic inverters, P/N ratio trade-offs, early input optimization, applications: wide NORs, datapaths, dual-rail vs. single-rail choices, control; multiple-output dynamic logic case study, Zipper domino, special purpose circuit families, bad circuit families, sense-amps & balanced circuits, CVSL, low-threshold circuits (NCMOS, pass transistors, general gates), circuit pitfalls: charge sharing, noise margins, process corners impacting ratios, threshold & V_{BE} drops, leakage, back driving, hot electrons, static timing analyzer limitations

Readings:	Logical Effort Ch. 10, 12, W&E Ch. 5.4.4-5.4.11
Handouts:	Signal & power network integrity
Assignments:	Problem Set 3
Tools:	Opus

S4: 3/12: Clocking & Latching

pipelining, static pipeline elements: ETFF, transparent latches, pulsed latches; performance implications: element delays, setup/hold times, clock skew, time borrowing; min-delay & solutions, wave pipelining, scan, global clock generation and distribution: single v. multiple phases, PLLs and DLLs, ad-hoc, grids, H-trees, and hybrid schemes; global skew: jitter, distribution sources; local clock generation and distribution: generator skew, wire skew; skew optimization: minimum delay, dummy loads, identical drivers, layout guidelines, driving middle of wires; asynchronous/self-timed circuits, delay generation and margining

Readings:	W&E Ch. 5.5 (this is a weak part of the text)
Handouts:	Alpha 21164 clocking, Survey I
Assignments:	Problem Set 4

S5: 3/19: High Performance Domino Design

textbook domino pipelines, performance limitations: latch delay, clock skew, time borrowing; skew-tolerant domino intro, skew-tolerant domino continued: local skew & time borrowing, interfacing with 1 and 2-phase static logic, scan, timing types

Handouts:	Skew-tolerant domino paper & slides, Skew-tolerant domino scan
Assignments:	Problem Set 5

S6: 3/26: Midterm

S7: 4/2: Arithmetic Unit Design

full adders, 4:2 compressors, multiple-input adders, ripple carry adders, carry lookahead/bypass, carry select, logarithmic structures, Ling adder, applications, multipliers

Readings:	W&E Ch. 8.2.1, 8.2.7
Handouts:	HP Ling adder
Assignments:	Project Description

No Class 4/9

S8: 4/16: Interconnect Engineering & Physical Design

fabrication process, layout design rules, gate layout strategies, metal planning, device parasitics, folding transistors, datapaths, random logic, arrays, floorplanning, area estimation, interconnect length estimation, significance of interconnect, wire resistance, wire capacitance models, RC delay lumped approximations to distributed lines, limitation of approximation, capacitive crosstalk, miller effect, interconnect width, spacing, interleaving signals, repeaters, IR drops, power grid integrity, inductance, interconnect RV: electromigration, self-heating

Readings: W&E Ch. 3, 4.3.5-4.4
Handouts: Layout Design Rules
Assignments: Project Presentation Guidelines

S9: 4/23: Array and Low Power Design

SRAM introduction: architecture, core cell, decoders & sizing, column circuitry, banking, multiple ports; ROMs, CAMs, array built-in self test, PLAs: architecture, self-timing, integration with dynamic pipelines, applications, voltage, frequency, and activity factor, no silver bullets, distribution of power consumption, minimize clock loads, shut down unused units, domino power reduction, dynamic voltage and frequency adjustment, exploiting parallelism, tolerating high power

Readings: W&E Ch. 8.3
Handouts: Chappell SRAM

S10: 4/30: Project Presentations & Wrapup

presentations, summary of key ideas for GHz design

Handouts: Survey II