High Speed CMOS Circuit Design

Problem Set 4

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1.0 Clocking Overhead

You are considering one of three clocking schemes for a static implementation of the Motoroil 68W86 processor: flip-flops, transparent latches, or pulsed latches. You expect that the adder self-bypass loop shown in Figure 1 will be the most critical path.

Suppose that the maximum delay of the adder is 8 FO4 delays, the result mux is 2 FO4 delays, and the bypass mux is 2 FO4 delays. Suppose the system has clock skew of 2 FO4 delays.[1]

1. Self-bypass paths see less skew than many other paths because the path starts and ends at the same sequential element. Nevertheless, we'll conservatively budget the same skew to all elements on the chip.

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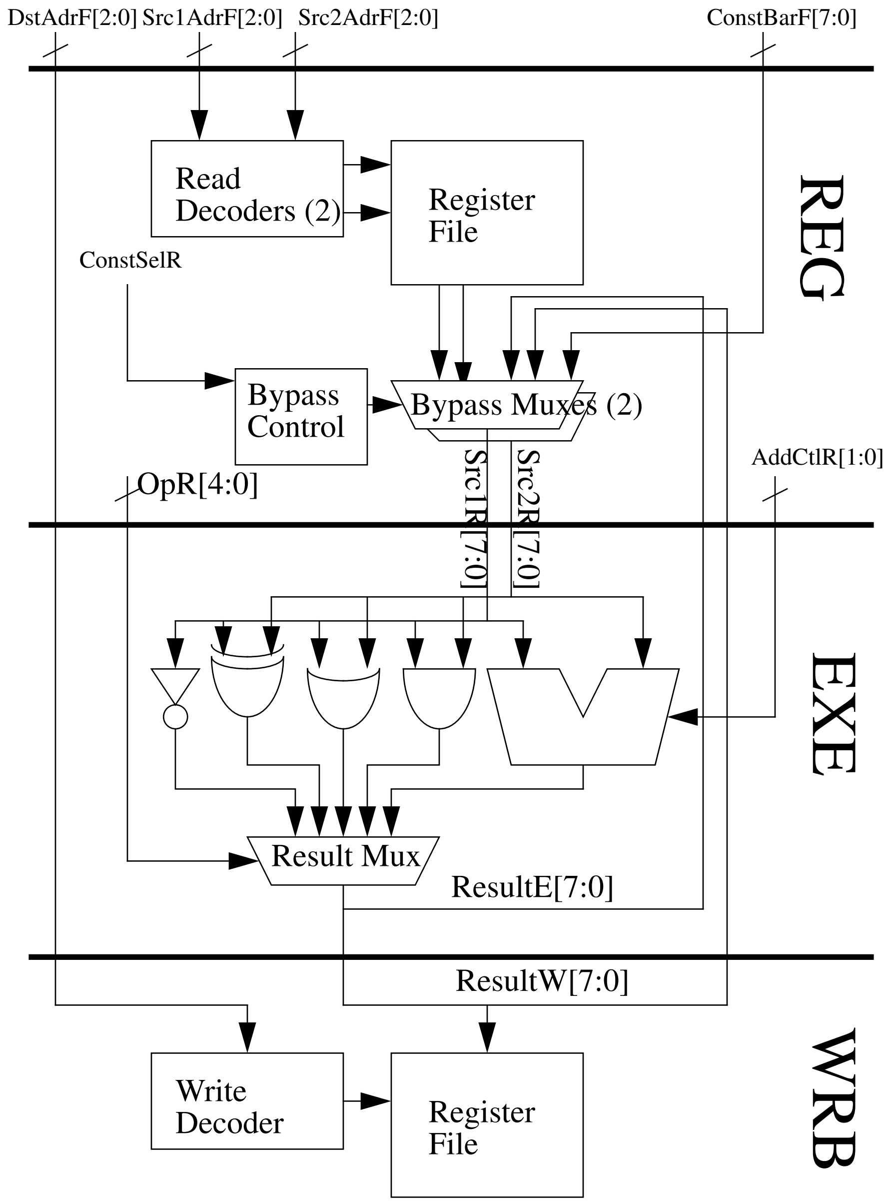
FIGURE 1. Motoroil 68W86 Pipeline Diagram



a) Suppose that a flip-flop has a setup time of 1.5 FO4 delay, a hold time of 0 FO4 delays, a maximum propagation delay of 1.5 FO4 delays, and a minimum propagation delay of 0.5 FO4 delays. What is the cycle time of the adder self-bypass path built using a flip-flop at the start of the cycle.

b) Suppose that a transparent latch has a setup time of 1 FO4 delay, a hold time of 0 FO4 delays, a maximum propagation delay of 1.5 FO4 delays, and a minimum propagation delay of 0.5 FO4 delays. What is the cycle time of the adder self-bypass path built using transparent latches in each half-cycle. You may assume that the logic can be broken into pieces which conveniently fit between each latch.

c) Suppose that a pulsed latch has the same delays as a transparent latch. Also suppose you use the shortest pulse necessary to hide all overhead. What is the cycle time of the adder self-bypass path built using a pulsed latch at the beginning of the cycle? How wide must your pulse be?

d) Using the result of Jobwork 3, compute the maximum operating frequency (in GHz) of each of the three designs (a-c). Which do you prefer? Why?

2.0 Min-Delay

If a cycle contains too little logic, a result may race through and violate the hold time of the clocked element at the end of the cycle.

Using the same delays from the previous question, find the minimum necessary contamination delay through logic in any cycle for:

a) flip-flop system

b) transparent latch system

c) pulsed latch system using the pulse width you chose in problem 1

3.0 Logical Effort

Do the following problems from the logical effort text to practice some of the advanced ideas in logical effort and begin reviewing for the midterm:

8-44, 8-45, 10-54, 10-55, 10-58