High Speed CMOS VLSI Design

Problem Set 1

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The objective of this assignment is to practice using the RC models of transistors to estimate gate delay and to optimize gate topology without resorting to simulation.

Remember that you are encouraged to discuss your answers with other engineers, but that your work should be your own. This assignment is due in the next class.

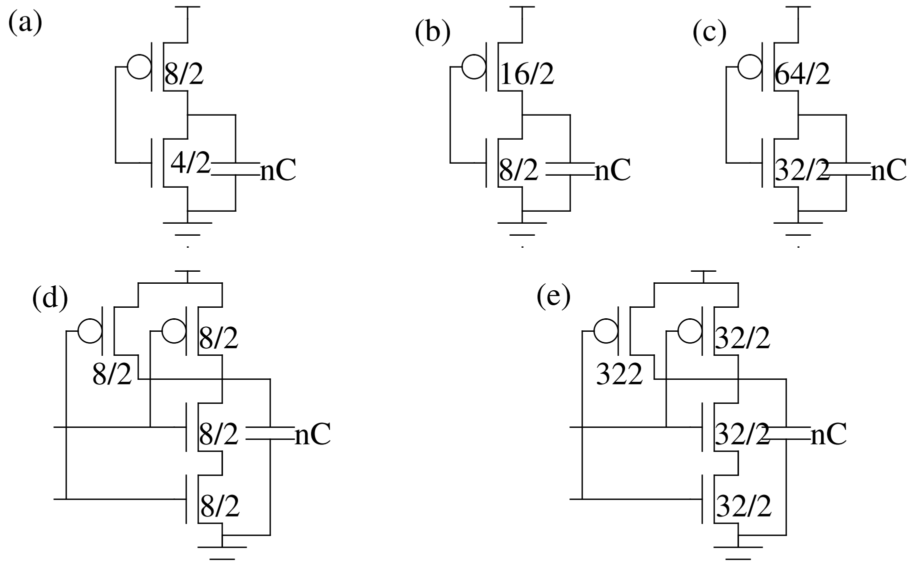
1: Logical Effort Problems

Do problems 1-1, 1-3, 2-9, 4-22

2: Gate Delay Estimation

Use the RC delay models presented in class to estimate the delay of each of the following gates. Express your results in terms of $\tau = RC$. As in class, assume that a unit (4/2) transistor has a gate capacitance C and a diffusion capacitance of C for contacted diffusion or C/

2 for uncontacted diffusion. A unit NMOS transistor has resistance R and a unit PMOS transistor has resistance 2R. Each gate drives a load of nC (where n is a variable).



3: Complex Gate Sizing

(a) Sketch an OAI gate (i.e., a gate that computes $\overline{(A+B)*C}$).

(b) Size the transistors so that the resistance through any pulldown or pullup path is R.

(c) Estimate the delay of the gate driving a load of nC.

4: Design Project: Wide AND Gate Design

Consider two ways to build an N-input AND gate. One is to build an N-input NAND gate, followed by an inverter. Another is to build two ~ N/2 input NAND gates followed by a 2-input NOR gate (for example, a 5-input AND could be constructed from a 2 and a 3-input NAND followed by a 2-input NOR).

Suppose the AND gate has a fanout of f, meaning that the load capacitance the AND gate drives is f times as large as the capacitance on the most heavily loaded AND gate input. Choose which of the two designs is fastest. Your answer should depend on N and f.

There will be a prize for the person who comes up with a correct answer and clearly explains it to the class.