High Speed CMOS VLSI Design

Project Description 2

Here's an update on the multiplier project, including a modified wire pitch specification and details on project milestones.

1: Milestones

4/16: 1 page write-up describing what architecture you plan to use and what the critical path is expected to be

4/23: 1 page write-up of preliminary critical path simulation results

4/30: Project presentation and report

2: Project Presentation

Plan to give a 5-10 minute presentation on the last day of class. You will need to explain what architecture you chose, what circuits and clocking techniques you are using, and what the critical path is. Discuss any interesting techniques you used. What is your cycle time?

After your presentation, other engineers will have a chance to ask questions, so make sure you can justify your conclusions.

3: Project Write-up

The project will be graded on six criteria: your 1-page milestone write-up, your project presentation, your architecture, modeling of the critical path in the architecture, circuit and clocking style, simulation / estimation technique, and final write-up. The purpose of the final report is to explain the important aspects of the design and methodology you used to convince me that your design will work.

The final report should explain how you arrived at your design. It is not just a notebook containing hard copies of all your SPICE output; rather it should be the kind of document you would give to other designers at a design review. The intended audience are experienced circuit designers, but they haven't been working on this project.

Your report must not only explain design decisions; it must also justify the models you used to simulate the design. Good modeling is as important as a good design.

Strive to make your report concise. Of course brevity is no excuse for a poorly written or confusing report; the reader has to be able to understand what you are trying to communicate. The length should satisfy 1 < (Number of Pages) < 20; I will not read more than 20 pages.

Suggested outline:

1. Overview description; choice of basic architecture, circuit style, clocking & latching method; assumptions made about timing; other assumptions; key circuit issues
2. Chip architecture and layout plan. What architecture did you choose for your multiplier, and what were the important advantages / disadvantages of this method? What function blocks does this method require and where are they placed in the layout. What is the general layout plan, and where are the long wires located. Estimate wire lengths.
3. Detailed circuit description. For each of the important circuits, state what was done and why. Also include other design possibilities and show why yours is better, if possible. Some choices are obvious, though.
4. Modelling. How were the simulation models generated. What values were chosen for wire loading and why? What paths were simulated, and why were these paths taken. Simulation results using these models.
5. Confidence level. In your opinion will the design that you report actually work? What nagging questions haven't you answered? What additional simulations should have been run?
6. Summary: overall performance, layout area, key ideas

4: Layout

The datapath pitch has been changed to 120 lambda to give you more freedom. Remember that the contacted metal pitch is 8 lambda and that you have 3 metal layers available.

You can estimate area, in square lambda, as 6 * gate area + 360 * number of transistors. This will help you estimate cell widths.

This estimate is only valid if all wires fit on top of the cell in the 120 lambda pitch. If you need extra routing, you must budget for it and include it in your calculations. Also, all wiring channels that run in M1 perpendicular to the dataflow must be explicitly considered, since they tend to block transistors.

5: Architecture

If you have a good architecture already, congratulations. If you are still struggling to understand multiplier architectures, this section may help.

Another Verilog model of a linear array multiplier is on the web page. It's not a particularly good array, but it's good enough for a design specification if you are running out of time. It also shows how to create the rounding logic without doubling the array area.

6: Modeling & Simulation

Remember that your objective is a feasibility study, estimating critical path delay and total area. You do not need to draw and simulate every cell in the multiplier. Instead, you need to develop a good model of the critical path and simulate just that path. Keep the model as compact as possible to minimize the wait for simulation.