EE371 Ersatzco Technology Overview

We will be using the Ersatzco 0.8 micron process models for EE371. The process is fairly primitive by current standards, so we have added a fourth layer of metal for your convenience. This document summarizes handy electrical characteristics of the process:

Interconnect

The process is planarized, so we will assume wire geometries are independent of the contents of other layers. Diffusion and poly are salicided for low resistance. Four metal layers are available; the first three are on a tight pitch, while the top layer is thicker and wider for power and critical global signals. The cross-section below shows wire thicknesses and dielectric spacings. Also, minimum wire pitch and sheet resistance are tabulated.

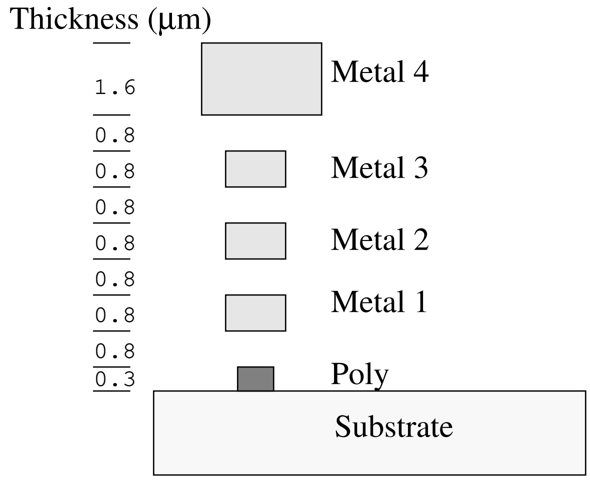

TABLE 1. Minimum Wire Pitch ($\lambda = 0.4\ \mu m$)

Layer	Width (λ)	Spacing (λ)
Poly	2	2
Metal 1	3	3
Metal 2	4	3
Metal 3	4	3
Metal 4	8	8

TABLE 2. Sheet Resistance

Layer	Sheet Resistance (Ω/square)
Poly	2.6
N-diffusion	2.4
P-diffusion	2.1
Metal 1/2/3	0.04
Metal 4	0.02

Contact resistance is 3 Ω between metal and poly or diffusion and 0.6 Ω between metal layers.

Electromigration reliability concerns allow a maximum of 1 mA/μm^2 of DC current through any metal line.

Extensive data about wire capacitance is available on the class web page.

Transistors

You will characterize transistors in PS2. BSIM models are used for more accurate modeling of short-channel devices. The BSIM models use curve-fit data rather than analytical transistor models. Data for fast, nominal, and slow process corners are available. Transistor models are located on the class web page.

Handy Physical Constants

Resistivity of Al @ 22C: 2.8 μΩ-cm

Permittivity of Free Space ε: 8.85e-14 F/cm

Dielectric Constant of SiO2 ε_r: 3.9

Speed of Light in Free Space: 3.0e8 m/s