High Speed CMOS VLSI Design

Syllabus

Instructors:

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Attendance:

Attendance is mandatory. In order to pass the class, you must attend at least 18 of the 20 sessions.

Assignments:

The only way to really learn anything is to do it. At each class, an “jobwork” will be given to practice the material. It is due at the following class. Your managers are aware that you will need to devote 2-3 hours of work time to the assignment; thus it is called “jobwork” instead of homework. If you find the assignments are taking longer than that, please let the instructors know so we can keep the workload reasonable. **Assignments are mandatory.** You may, however, skip up to two assignments and still pass the class. You are encouraged to discuss ideas with other engineers, but must turn in your own solutions, not a photocopy of a group solution. In the final weeks, the assignments will become a team project involving the design of a blindingly fast 8-bit microprocessor. There are no exams.

Detailed Schedule:

Class meets from 9-11 two days a week (Monday & Wednesday or Tuesday & Thursday) for 20 sessions. In general, the first 20 minutes will be dedicated to discussion of the previous day's assignments. There also will be a 5 minute break to stretch or imbibe caffeine.

9/3-9/4: Circuit Refresher Sessions

9/5: Microarchitecture Refresher

S1: 9/8-9: Circuits Introduction, Gate Delay Modeling

Logistics, designing for speed on the back of an envelope, RC models of transistors, application to gate delay, limitations of RC models: input slope, velocity saturation, tapered buffer chain sizing, fanout-of-4 (FO4) inverters, FO4 delay metric

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S2: 9/10-11: Gate Sizing & Logical Effort

optimal P/N ratio of inverters and other gates, sizing of other gates, logical effort, gain-of-4 rule, general logical effort sizing methodology, examples

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S3: 9/16-17: Sizing & Simulation

delay allocation sizing methodology, comparison to logical effort, simulation techniques, extracting parameters for back of the envelope calculation, curve-fitting gates to RC models, minimizing use of simulation

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S4: 9/18-19: Microarchitecture I: Arch vs. uArch

S5: 9/22-23: Interconnect RC

significance of interconnect, wire resistance, wire capacitance models, RC delay lumped approximations to distributed lines, limitation of approximation, capacitive crosstalk, miller effect, interconnect width, spacing, interleaving signals, repeaters

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S6: 9/24-25: Interconnect Scaling, Inductance

interconnect scaling, trends, inductance: physical origins, di/dt noise, inductive crosstalk, on-chip parasitic solenoids, impacted structures, inductance extraction, design solutions: ground planes, interdigitated power lines, interdigitated busses

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S7: 9/29-30: Static Circuit Families

CMOS gate design: NAND/NOR issues, complex gates, skewed gates, logical effort revisited, early input optimization, stack height, tapered stacks & related fallacies; transmission gates: applications, P/N ratio, logical effort, series gate limits, NMOS-only vs. transmission gates, level restoration, noise margins, complementary pass transistor circuits, other pass transistor variants; pseudo-NMOS: review of NMOS, gate design, logical effort, drawbacks: noise margins, power consumption, ratio problems across process; solutions: IDDQ mode, current mirrors; symmetric NOR gates

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S8: 10/1-2: Dynamic Circuit Families

Dynamic gate topology, skewing gates, series evaluation devices, advantages: speed, area, challenges: monotonicity, charge sharing, crosstalk, noise margin, subthreshold leakage; solutions: domino, dual-rail circuits (DCVS), self-timing, posponing nonmonotonic functions, intermediate precharge devices, shielding, keepers; logical effort, gain effects of dynamic inverters, P/N ratio trade-offs, early input optimization, applications: wide NORs, datapaths, dual-rail vs. single-rail choices, control; multiple-output dynamic logic case study, Zipper domino

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S9: 10/7-8: Special Purpose Circuit Families & Circuit Pitfalls

special purpose circuit families, bad circuit families, BiCMOS, sense-amps & balanced circuits, CVSL, low-threshold circuits (NCMOS, pass transistors, general gates), DSL, pitfalls: charge sharing, noise margins, process corners impacting ratios, threshold & V_{BE} drops, leakage, back driving, static timing analyzer limitations

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S10: 10/9-10: Microarchitecture II: Branch Prediction

S11: 10/13-14: Static Pipeline Design, Latching Strategies

pipelining, static pipeline elements: ETFF, transparent latches, pulsed latches; performance implications: element delays, setup/hold times, clock skew, time borrowing; min-delay & solutions, wave pipelining, scan

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S12: 10/15-16: Dynamic Pipeline Design

textbook domino pipelines, performance limitations: latch delay, clock skew, time borrowing; skew-tolerant domino: local skew & time borrowing; interfacing with static logic, scan

S13: 10/20-21: Clock Generation & Distribution, Self-Timing

global clock generation and distribution: single v. multiple phases, PLLs and DLLs, ad-hoc, grids, H-trees, and hybrid schemes; global skew: jitter, distribution sources; local clock generation and distribution: generator skew, wire skew; skew optimization: minimum delay, dummy loads, identical drivers, layout guidelines, driving middle of wires; self-timed circuits, delay generation and margining, zero-overhead self-timing, pitfalls

S14: 10/22-23: Adder Design

full adders, 4:2 compressors, multiple-input adders, ripple carry adders, carry lookahead/bypass, carry select, logarithmic structures, Ling adder, applications

S15: 10/28-29: Array Design

SRAM introduction: architecture, core cell, decoders & sizing, column circuitry, banking, multiple ports; ROMs, CAMs, array built-in self test, PLAs: architecture, self-timing, integration with dynamic pipelines, applications

S16: 10/30-10/31: Microarchitecture III: Advanced Processor Techniques

S17: 11/3-4: Divider Design

dividers as a case study in high speed circuit design; review of division, SRT division, divider architectures, divider circuits, sizing example, floorplanning, performance results

S18: 11/5-6: Low Power Design

voltage, frequency, and activity factor, no silver bullets, distribution of power consumption, minimize clock loads, shut down unused units, dynamic voltage and frequency adjustment, exploiting parallelism, tolerating high power

S19: 11/10-11: Project Presentations & Circuits Wrapup

presentations, summary of key ideas for GHz design

S20: 11/20-21: Microarchitecture IV