High Speed CMOS VLSI Design

Problem Set 7

The objective of this assignment is to apply your skills at dynamic logic design to build a fast full adder.

Readings:

- Skim sections 5.4.4-5.4.11 of W&E.

1.0 Dynamic Adder Design

Design an full adder using dynamic logic to meet the following block specification:

- **Inputs**: A_h, A_l, B_h, B_l, Cin_h, Cin_l (maximum of 5 microns gate load on each)
- **Output**: S_h, S_l, Cout_h, Cout_l (drive 5 microns of gate load each)
- **Function**: `{Cout, S} = A + B + Cin`
- **Delay**: minimize $t_{Cin->Cout} + 1/2\ t_{any\ input->S}$

The inputs and outputs are monotonically rising dual-rail signals. A_h rises to indicate that A is 1. A_l rises to indicate that A is 0. When A_h and A_l are both low, the circuit is pre-charged and idle. Delays should be measured from either input changing to the latest of the _h or _l output rising.

Simulate your circuit under the same voltage and temperature you used in Jobwork 3. Let your inputs be driven by ramps with 20-80% rise times equal to that of a FO4 inverter (i.e. 1.66 FO4 delay 0-100% ramps). Assume the clock arrives much earlier than the last data input.

If a full adder is used in a ripple-carry adder, the delay from Cin to Cout is most critical. Nevertheless, the delay from any input to S should not get unreasonably large. Therefore, the objective of this design is to minimize the weighted sums of these delays. Be sure to find the worst case input patterns when measuring delay. Report your answer both in pico-seconds and in FO4 delays, using the FO4 delay from the Jobwork 3 solutions. Also, report the speedup over your Jobwork 6 static design.

The objective is to minimize delay. However, use good judgement and do not let other factors such as area or power get out of hand. There will be a prize for the best convincing design.