High Speed CMOS VLSI Design

Problem Set 5

The objective of this assignment is to think about on-chip inductance and to apply what you have learned about repeaters to rapidly drive a long on-chip wire.

Readings:

- Read section 4.4 of W&E.
- Read the DEC and IBM papers about on-chip inductance

1.0 On-chip Inductance: Real or Hoax

John Bull builds an ASIC using entirely static gates. It computes the Mandelbrot set using billions of calculations, then stores the results in a bunch of flip flops. The results are shifted out a scan chain connected to the flops at 1 MHz. He decides not to bother with worrying about inductance, so he doesn't model it or even use any bypass capacitors on chip. John tests his chip and finds that it runs at 400 MHz in a 0.18 micron process. He concludes that inductance concerns are just a hoax. Is he right? Explain why, or what is wrong with his reasoning.

2.0 Repeater Design

You need to drive a signal 20 mm across the MegaHAL^{TM} chip as fast as possible. The first stage driver uses a total of 100 microns of transistor width. The load at the end of the line is 300 microns of transistor gate. The line carrying the signal has a resistance of 20 Ω/mm and a capacitance of 0.3 pF/mm.

a) Suppose you don't use any repeaters. (1) Estimate the delay of the circuit, using the values of R and C you found for your process. (2) Model the wire delay in HSPICE using 1, 2, 4, and 8 Pi sections.

b) Design a set of repeaters to get the signal across the chip as fast as possible. Simulate the wire delay in HSPICE. This is a design contest. There will be a prize for the fastest convincing design.