High Speed CMOS VLSI Design

Problem Set 4

The objective of this assignment is to explore the impact of wires on path sizing and delay and to look at failures caused by capacitive coupling and other wire problems.

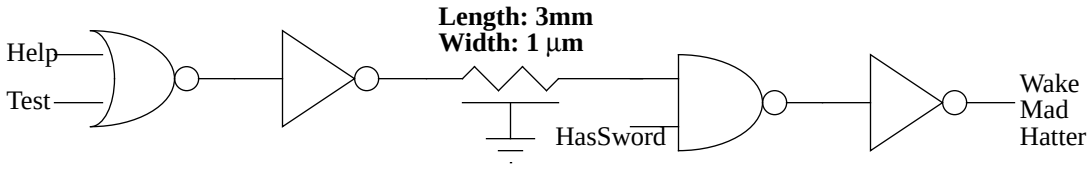
Readings:

- Read section 4.2 and 4.3.5-4.3.8 of W&E.

1.0 Sizing & Delay Estimation in Wonderland

Alice is trapped in Wonderland by the Queen of Hearts, who wants to cut off her head. She needs to send for help to the Mad Hatter, who can come to her help with a vorpal sword. Unfortunately, the Mad Hatter is sitting three millimeters away from Alice, so she decides to build a small integrated circuit to carry the call for help across the distance in as little time as possible. Being a good engineer, she also decides to include a test input (to allow calls to the Hatter even when there is no emergency) and to provide an override that prevents the Hatter from being paged when he doesn't have his sword handy and therefore cannot be of assistance (she'd hate to waste his time). Her circuit is shown below.

FIGURE 1. Alice's Rescue Circuit



Suppose the wire has a resistance of 0.05 Ω/❑ and a capacitance of 0.2 fF/μm. In the process she is using, gates have C = 2.0 fF/μm and R=5KΩ*μm. Since she is feeling weak, she can only power an input load of 12 fF. The Mad Hatter presents 1 pF of capacitance that must be driven to wake him.

a) Size the circuit to wake the Hatter quickly.

b) Estimate the delay of the circuit. If the queen is about to cut off Alice's head in 1.5 ns, will Alice get help in time?

2.0 Wire Cross-Cap

Ben Bitdiddle is designing the MegaHAL^{TM} Processor and requires a 64 bit bus to transfer data 3000 μm from the Level 1 Data Cache to the Integer Execution Unit. Since the path is critical, the bus is driven with dynamic logic: all lines are first precharged high, then some are pulled low. MegaHAL design methodology requires that all logic levels be within 30% of nominal (i.e. a logic 1 must have a voltage of VDD +/- 30%). Power supply variation is +/- 10% from nominal. Noise spikes on dynamic nodes should not bring the value outside of its valid logic level. Help Ben optimize the bus design.

Assume you are stuck in a primitive 0.8 micron process and refer to the capacitance tables mentioned in the lecture notes.

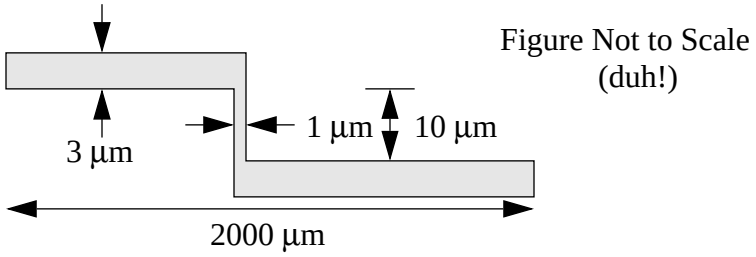
a) Suppose the bus is built in metal 2 with the substrate below and no wires above. Design the width and spacing of the wires to satisfy noise margins while minimizing area.

b) How would your answer change if there were solid grounded planes of metal 1 and metal 3 encasing the bus? Be quantitative.

3.0 Wire Failure

Dr. Hairless, an evil CAD tool developer, proposes a novel scheme for compacting wires in an automatic layout system. The system routes Metal 2 wires of a user-specified width and spacing horizontally across a datapath. It occasionally jogs the wire vertically with Metal 2 in order to eliminate wasted routing space. To minimize the area of the jogs, Dr. Hairless proposes using minimum width wire segments for the jog. He argues that as long as the length of the jog is much less than the length of the entire wire, total resistance and coupling will increase negligibly.

You are evaluating this CAD tool. In one test case, it routes a 2000 μm long signal which you specify to be 3 μm wide. Along the way, the tool introduces a 10 μm jog which is only 1 μm wide, as shown below:



a) Do you agree that the total resistance and coupling changes by a negligible amount?

b) Can you think of any other problems caused by this layout tool?