



High Speed CMOS VLSI Design

Project Presentation

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Your team should plan a 3-5 minute presentation of your FemptoHAL processor design. You should plan to convey the following information:

- status of your project
- microarchitecture optimization(s)
- overview of circuit design
 - adder architecture
 - how is the design partitioned into static and domino sections
 - any interesting tricks you used
- operating frequency

If your project is entirely done and passes all the HSPICE test vectors, you are in great shape. If you can't completely finish it, you should make a convincing argument that you have considered all the critical paths and that the operating frequency you claim is feasible. You should definitely connect the appropriate clock phases to gates and simulate several additions bypassing to each other so that any clocking overhead is revealed. Other common problems you should be sure you have addressed are:

- charge sharing unless secondary precharge devices are used on tall dynamic gates
- insufficient precharge time given size of precharge transistor and skew of static gate
- min-delay violations between pulsed latches or at static/domino interface
- monotonicity violations

After the presentations, the rest of the class will have an opportunity to further review the teams with the three fastest designs. A class vote will select the most convincing of the three for the prize!

If you are feeling behind schedule on the project, you are not alone. Unless you are trying to win the prize, focus maximizing the learning / time ratio of your effort: stop shaving picoseconds off your critical path and try to get a design that works correctly so you get the full experience of domino design and static/domino interface issues. A reasonable effort justifying your operating frequency will be enough to earn credit for the project.