

Reading: W&E Sections 8.2.1-8.2.6, 7.3.3

The first step of your FemptoHAL circuit work is to design and simulate the critical path. This will set the cycle time goal to which you will aim the rest of your circuits.

If you build all of your circuits well, the adder self-bypass path will probably be the longest single-cycle path. This is the path starting with the adder/subtracter, passing through the result multiplexor then bypass multiplexor, and returning to the adder inputs.

Design this path and simulate it to find the cycle time under worst-case input data. Your goal is to run the path as fast as possible. Notice that there are no capacitance specs because the path is a loop; increasing all gate sizes by 10x has no effect on speed because both input and output loading increases 10x. Be sure to include any logic optimizations you've developed while writing your Verilog.

There will be a prize for the team producing the fastest bypass path.