High Speed CMOS VLSI Design

Project Phase 1: Verilog Model

This assignment is the first step of the project. You should find a partner who is in the same section of the class. You will need to stick with your partner for the remainder of the project. Ideally, you should find a partner who complements your skills.

The goal of this assignment is to understand and optimize the microarchitecture of the FemptoHAL processor. To do this, you will code (and probably debug!) a model of the processor in Verilog. A basic template is provided; you need to complete it. The template has no optimizations for the critical path; you should plan to make at least one optimization and are welcome to implement as many as you can dream up.

Testvectors and an incomplete Verilog model of the FemptoHAL are in the class directory.

a) Copy these files to your home directory and complete the Verilog model. Run Verilog with the command: `verilog femptohal.v` and see if your program runs all the test vectors without any error messages. If you get dropped into the Verilog interactive mode, you can exit with ctrl-D. To debug your code, you may find it useful to add $display statements or to bring up a waveform viewer.Note that the instruction encoding in the test vectors file does not exactly match that in the project description. Ignore the description.

b) The microarchitecture is not particularly optimized for speed. Make at least one optimization to improve performance (you'll have to estimate what paths are likely to be critical). To improve your chance at winning the project prize, you may want to add as many optimizations as you can. Hint: is there any way to keep the adder result from having to pass through a five input result multiplexor? Turn in a paragraph or block diagram showing the optimization you made.