

# **1.0 Introduction**

We have seen that static sequential logic can be constructed using flip-flops, transparent latches, or pulsed latches. In this lecture, we will explore methods for building dynamic sequential logic. Then we will look at how to interface static and dynamic logic and how to support scan for both types of circuits.

# 2.0 Dynamic Sequential Logic

Dynamic pipelines are traditionally designed with static latches in each phase. Such a style proves to have huge overhead from clock skew, latch delay, and the inability to borrow time. The problems can be overcome by controlling domino logic with multiple overlapping clock phases.

This technique is described in the "Skew-Tolerant Domino Circuits" paper by Harris and Horowitz so will not be discussed further here.

## 3.0 Static/Dynamic Interface

Static and dynamic circuits may use different clocking schemes, so it is important to be able to send static inputs to dynamic logic blocks and dynamic inputs to static circuits in a low overhead fashion.

The interface of dynamic signals with transparent latch-based static logic is described in the "Skew-Tolerant Domino Circuits" paper. The interface of dynamic signals with pulsed-latch static logic is described in the "Domino Circuit Methodology" paper.

### 4.0 Scan

Testing chips is becoming very difficult. Traditional test techniques involved probing toplevel metal lines with a tiny metal probe or electron beam. As more layers of metal are used, most nodes of interest become blocked by the power, ground, and clock nets which occupy most of the upper levels of metal. Moreover, "flip-chip" packaging is rendering internal nets even more difficult to reach. The technique involves placing solder balls directly on top-level metal pads, then flipping the chip so the pads align with the package or board and heating the solder to make the connection. In such a style, the only way to probe metal lines on the chip is to physically drill or etch a hole through the back of the substrate! This is slow, expensive, and hard to do.

Thus, most designers use scan chains to test their chips. Flip-flops are connected into a chain with a special scan multiplexor so their contents can be marched through the chain instead of captured from a previous stage of logic, as shown in Figure 1. Each flop in the 3-bit datapath can receive data from a normal input or from the previous flop in the chain.

#### FIGURE 1. Flops connected in scan chain



Scan contributes nothing of value except ease in testing, so designers want to minimize its impact on the chip. In particular, a good scan system should feature:

- Zero increase in cycle time
- Zero design time
- Zero timing critical scan signals
- Zero extra area

Adding multiplexors to the critical path is usually unacceptable for speed. With a good scan methodology, the increase in cycle time is just a small amount of extra diffusion loading on latches or domino gates. The design time can be minimized with a clear and simple set of design rules worked out in advance and integrated into the library so designers don't have to concern themselves with scan. A good methodology also does scan with only a small number of scan signals, which may be operated arbitrarily slowly so poor routing and buffering of the scan signals doesn't degrade chip operation. Unfortunately, the area criteria is not met well; most scan schemes require extra "shadow latches." A scheme for scanning pulsed latches and domino is described in the "Domino Circuit Methodology" paper.