Introduction to Computer Architecture (E114)

Harris **Spring 1999**

Syllabus

Instructor

David Harris Parsons 374 x73623 David_Harris@hmc.edu

Schedule

Lecture: MWF 9-10 / 10-11
Office Hours: M11-12, T13-16, F11-12, or by appointment

Text

Patterson & Hennessy, *Computer Organization & Design*, 2nd Edition Morgan Kaufmann 1998

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e114
Class email list: eng-114-1-l / eng-114-2-l

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe <list-name> (where you choose section 1 or section 2)

Grading

Labs: 25%
Problem Sets: 20%
Participation: 5%
Midterms: 15% each
Final: 20%

Late labs and homework will not be accepted. Your lowest lab and homework score will be dropped before the average is calculated. You are welcome to discuss labs and problem sets with other students or with the instructor **after** you have made an effort by yourself. However, you should turn in your own work, not work identical to that of another student. **It is an honor code violation to simply copy someone else's work.**

Tentative Schedule

The following schedule is a tentative plan that may change during the semester. The deadlines, however, are fixed unless otherwise notified; *do not assume* that they will change just because the lecture schedule changes.

Date	Reading	Lecture	Deadlines
W0			
20-Jan	1.1-1.8	Introduction: Digital Abstraction & Static Discipline	
22-Jan		Truth Tables and Logic Gates	
W1			
25-Jan	B1-2	Boolean Expressions and Algebra	
27-Jan		Dynamics: timing issues, hazards, K maps	Lab 1 due
29-Jan	B4-5	Sequential blocks: RS latches, D latches, flops, clocking	Problem Set 1 due
W2			
1-Feb	B6	Finite State Machines	
3-Feb	B7	Timing constraints: setup, hold, prop, cont, metastability, synchronization	Lab 2 due
5-Feb		Building blocks: muxes, decoder, priority encoders, counters, shift regs	Problem Set 2 due
W3			
8-Feb	B3	ROMs, PLAs, RAMs, FPGAs	
10-Feb	4.1-4.2	Number Systems: fixed and floating point, positive & negative	Lab 3 due
12-Feb	4.3-4.5	Arithmetic: addition & subtraction	Problem Set 3 due
W4			
15-Feb	4.6, 4.8	Arithmetic: multiplication	
17-Feb		Midterm	First Midterm
19-Feb		<slop>	
W5			
22-Feb	3.1-3.4	Instruction Set, Registers	
24-Feb	3.5-3.6	Branches & Calls	Lab 4 due
26-Feb	3.7-3.8	Addressing Modes	Problem Set 4 due
W6			
1-Mar	3.9-3.15	Arrays & Pointers	
3-Mar	2.1-2.9	Performance measurement	Lab 5 due
5-Mar		Verilog Modeling	Problem Set 5 due
W7			
8-Mar	5.1-5.2	Building datapaths	
10-Mar	5.3, C1-2	Generating control	Lab 6 due
12-Mar	5.4, C3	Multicycle implementation	Problem Set 6 due
W8		Spring break	R & R
W9			
22-Mar	5.5, C4-6	Microprogrammed control	
24-Mar		Emulation, x86 uops	Lab 7 due
26-Mar	5.6-5.10	Exceptions	Problem Set 7 due
W10			
29-Mar	6.1-6.3	Pipelining	
31-Mar	6.4-6.7	Pipeline hazards, stalls	Lab 8 due
2-Apr	7.1	Memories: latency & throughput	Problem Set 8 due
W11			
5-Apr	7.2-7.3	Caches	
7-Apr		Second Midterm	Second Midterm
9-Apr	7.4	Virtual Memory	
W12			
12-Apr	7.5-7.9	Memory Hierarchy	
14-Apr		FPGAs, ASICs, Custom Chips	Lab 9 due
16-Apr	8.1-8.4	I/O: Busses, polling & interrupts, memory mapping, performance	Problem Set 9 due
W13			
19-Apr	8.5-8.10	I/O: File systems	
21-Apr		Operating systems: processes	Lab 10 due
23-Apr		Operating systems: synchronization & communication, semaphores	Problem Set 10 due
W14			
26-Apr	9.1-9.4	Parallel processing	
28-Apr	9.5-9.10	Parallel programming	Lab 11 due
30-Apr	6.8	Advanced architecture: superscalar, dynamic execution	Problem Set 11 due
W15			
3-May	6.9-6.12	Case study: Pentium II	
5-May		Architecture trends	Design Competition