Introduction to Computer Engineering (E114)

Harris Spring 1999

Problem Set 7 **Due: Friday, March 26**

Reading: Chapter 5.1-5.4, Appendix C1-C3

1) Adding Instructions to a Single-Cycle Processor

Ben Bitdiddle needs the `lui` instruction for his MIPS processor. Extend the single-cycle processor from Section 5.3 to handle `lui`. Attached is Figure 1 showing the single-cycle datapath. If you need to modify the datapath, mark your modifications on the figure. If not, leave the figure unmarked. Then add a row to the table below showing control signals that must be asserted. If you need any additional control signals, add another column to the table.

Op[5:0]	Instruction	Control Outputs								
		RegDst	ALUSrc	MemtoReg	RegWrite	MemRead	MemWrite	Branch	Jump	*ALUOp[1:0]*
000000	R-type	1	0	0	1	0	0	0	0	***10***
100011	lw	0	1	1	1	1	0	0	0	***00***
101011	sw	X	1	X	0	0	1	0	0	***00***
000100	beq	X	0	X	0	0	0	1	0	***01***
000010	j	X	X	X	0	0	0	0	1	***00***
	lui									

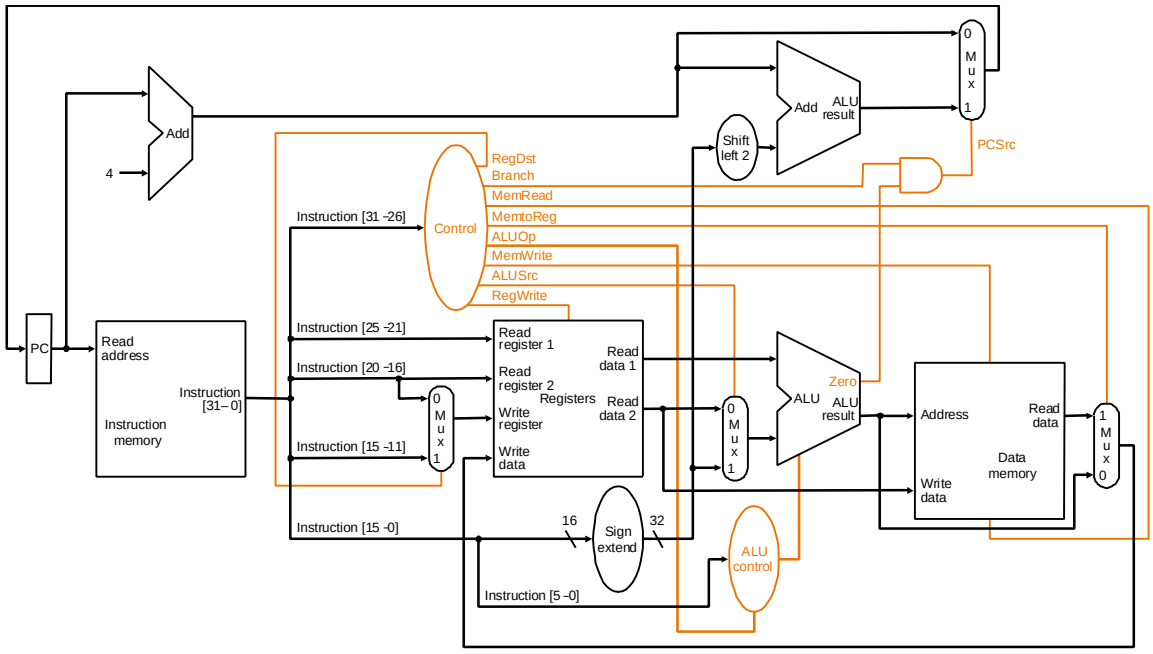

Figure 1: Single-Cycle Datapath

2) Adding Instructions to a Multi-Cycle Processor

Now Ben would also like to use the `lui` instruction in his multi-cycle MIPS processor. Extend the multi-cycle processor from Section 5.4 to handle `lui`. Attached is Figure 2 showing the multi-cycle datapath. If you need to modify the datapath, mark your modifications on the figure. Then change the Finite State Machine in Figure 3 to produce the required control signals at the right times.

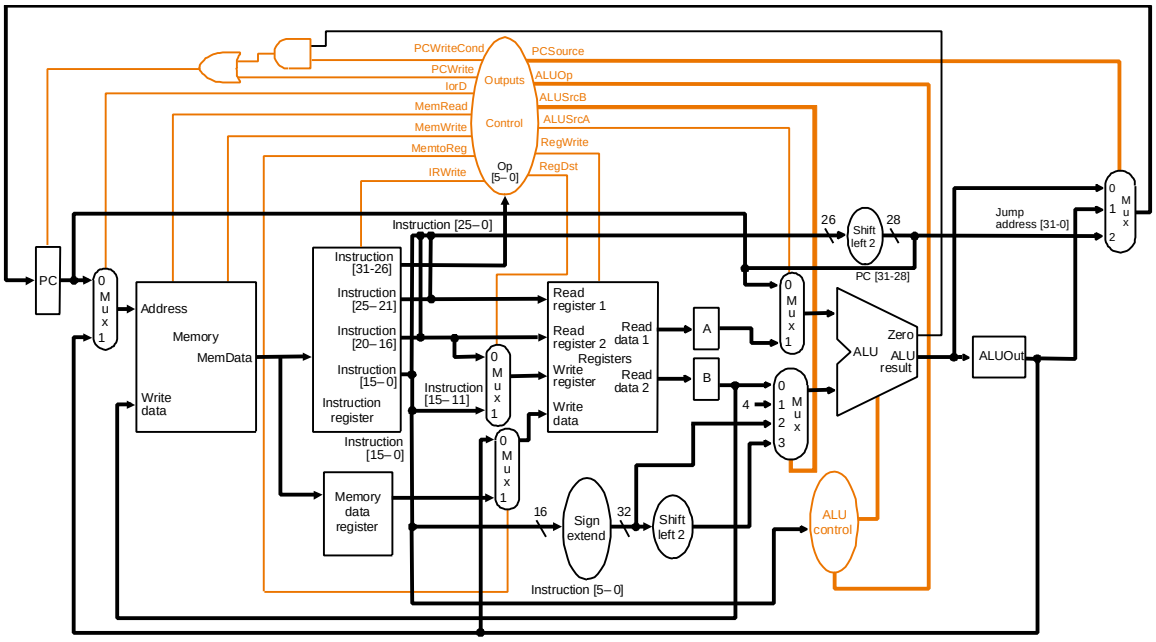

Figure 2: Multi-Cycle Datapath

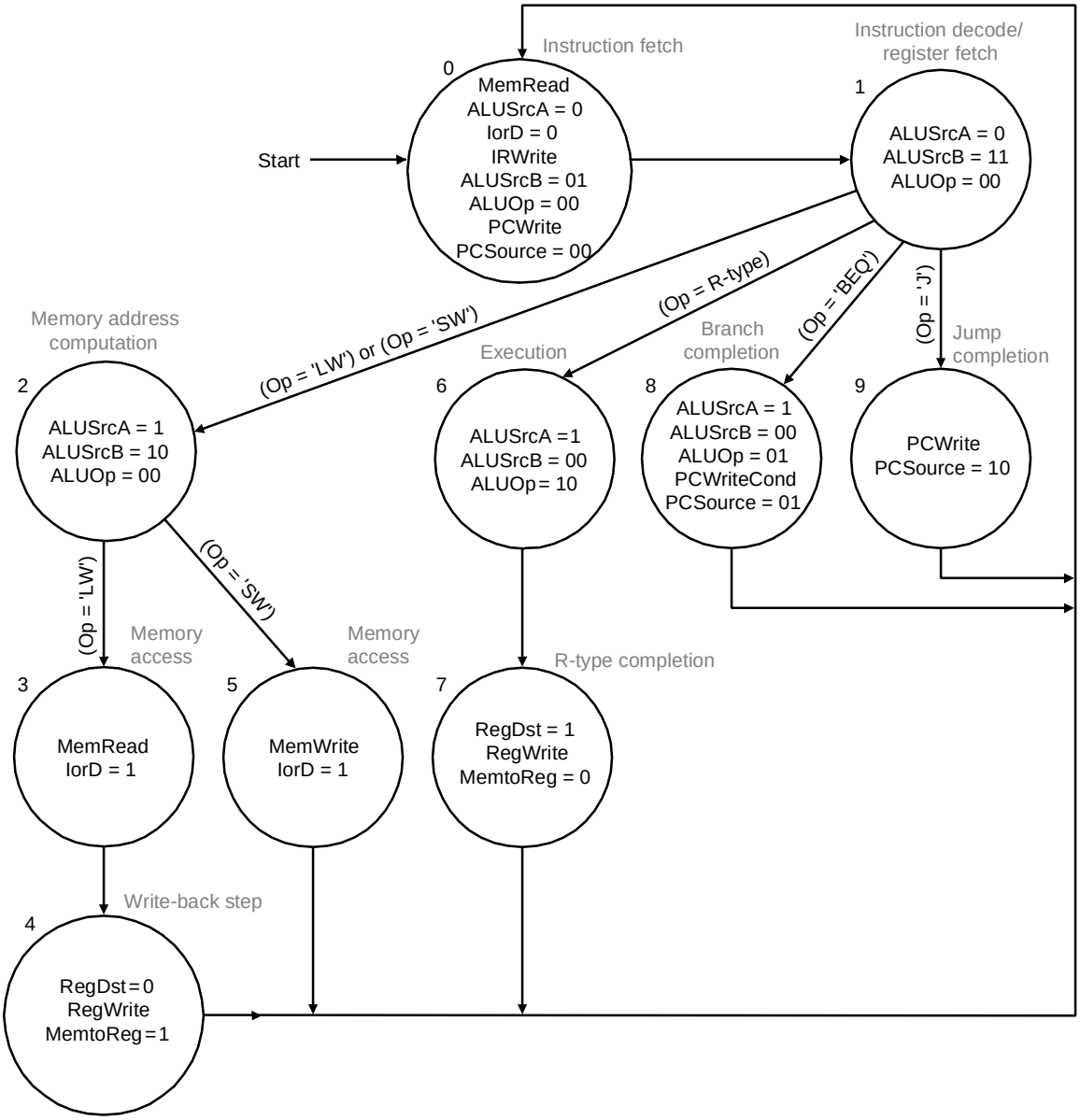

Figure 3: Multi-Cycle Control

3) Time

Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for next semester's class.