Introduction to Computer Engineering (E114)

Harris Spring 1999

Problem Set 3 **Due: Friday, February 12**

1) Timing Analysis

The figures below illustrate two versions of a digital system. Both start with flip-flops and contain four blocks of combinational logic with indicated delays. The top system uses D flip-flops internally, while the bottom system uses D-latches. Assume the clocked elements have the following timing specs:

	D Flip-Flop	D Latch
Δ_{CQ}	100 ps	100 ps
δ_{CQ}	60 ps	60 ps
Δ_{DC}	80 ps	80 ps
Δ_{CD}	20 ps	20 ps
Δ_{DQ}	N/A	70 ps

a) If there is no clock skew, how fast can the system operate (in MHz)? When does data arrive at each point x_i, relative to the rising edge of clk?

b) If the clock runs at 800 MHz, how much clock skew can each system handle before setup times are violated?

c) If the system is operated at 1 Hz, how much clock skew can each system handle before hold times are violated?

2) Synchronization

Consider two ways of building a synchronizer of an asynchronous input X. We define system failure if the input to the last flip-flop is metastable when it is sampled on the rising edge of the clock. The first method waits 2 cycles before examining the data and operates at 1 GHz. The second method waits only 1 cycle before examining the data but is clocked at only 500 MHz. The delays of the flip-flops are the same as given in problem 1. A=10; τ = 30 ps. Suppose the transition time of the input X is 100 ps.

What is the MTBF of each system if the arrival time of X is a uniformly distributed random variable?

3) Time

Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for next semester's class.