Introduction to Computer Architecture (E114)

Harris Spring 1999

Problem Set 1 **Due: Friday, January 29**

1) Static Discipline

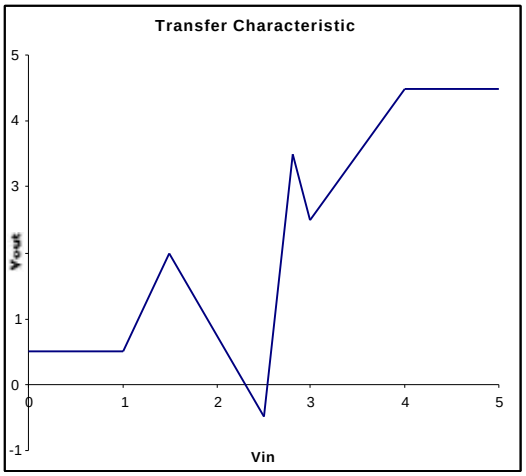

Figure 1

Is it possible to assign valid logic levels and noise margin boundaries so that a device with the transfer characteristics shown in Figure 1 would serve as a buffer? If so, what are the input and output high and low levels (V_{ol}, V_{il}, V_{ih}, and V_{oh}) and noise margins?

2) Truth Tables

Prove that the 2-input NAND gate is universal by using such gates to construct AND, OR, NOT, and XOR gates? How few NANDs do you need to construct XOR?

3) Time

Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for next semester's class.