SiFive FE310-G003 Datasheet
1.0.1

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SiFive FE310-G003 Datasheet

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Release Information

Version	Date	Changes
1.0.1	March 25, 2021	Added Creative Commons license
1.0.0	July 27, 2020	Initial Datasheet Release

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Chapter 1

FE310-G003 Description

Features

- SiFive E31 Core Complex.
- Flexible clocking options including internal PLL, free-running ring oscillator and external 16MHz crystal.
- 1.61 DMIPs/MHz, 2.73 Coremark/MHz
- RV32IMAC
- 8kB OTP Program Memory
- 16kB Instruction Cache
- 64kB Data SRAM
- 3 Independent PWM Controllers
- External RESET pin
- JTAG, SPI, I2C and UART interfaces.
- QSPI Flash interface.
- Requires 1.8V and 3.3V supplies.
- Hardware Multiply and Divide

Description

The FE310-G003 is built around the E31 Core Complex instantiated in the Freedom E300 platform.

The *FE310-G003* manual should be read together with this datasheet. This datasheet provides electrical specifications and an overview of the FE310-G003.

The FE310-G003 implements full production test and will be offered as fully qualified and tested parts in produciton quantities. Please consult with SiFive marketing for schedule and specification.

The FE310-G003 comes in a convenient, industry standard 6x6mm 48-lead QFN package (0.4mm pad pitch).

Chapter 2

FE310-G003 Pins

FE310-G003 Pinout

The FE310-G003 is offered in a convenient 48-lead 6x6 QFN package (0.4mm lead pitch). The exposed paddle (Pin 49) must be connected directly to the ground plane.

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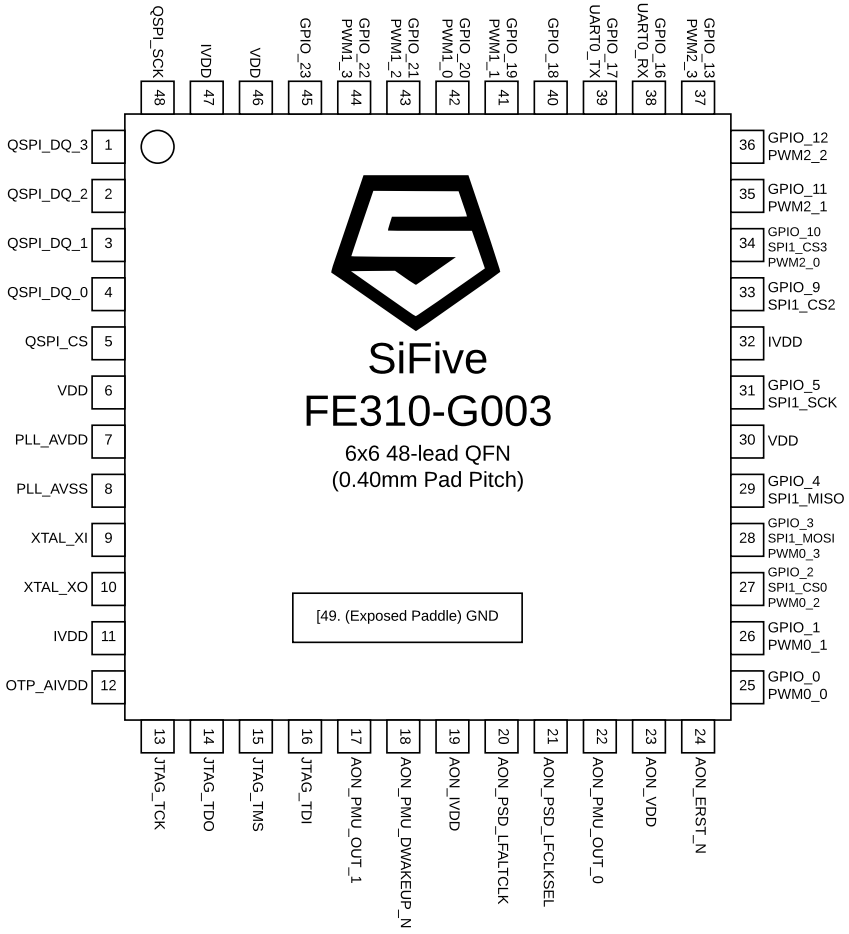

Figure 2.1: FE310-G003 Pinout

Pin Descriptions

Power Pins

VDD (6, 30, 46) : Core supply voltage. 1.8V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

IVDD, AON_IVDD (11, 19, 23, 32, 47) : I/O and AON supply voltage. 3.3V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All IVDD pins must be connected externally.

OTP_AIVDD (12) : OTP supply voltage. 3.3V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All IVDD pins must be connected externally.

PLL_AVDD (7) : PLL supply voltage. 1.8V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

PLL_AVSS (8) : Isolated PLL supply bypass. Connect through a 1uF ceramic capacitor to PLL_AVDD. This pin is not to be connected directly to GND.

GND (49) : Exposed paddle is a ground return and must be connected directly to the ground plane.

Crystal Drivers

XTAL_XI (9) : 16MHz Crystal Input
XTAL_XO (10) : 16MHz Crystal Output

An external 16MHz crystal may be connected between the two XTAL pins. The crystal should have a capacitive load of 12 pF and an ESR 80 Ohms. An external oscillator may also be used to drive the FE310-G000 through the XTAL_XI input, in which case the XTAL_XO pin should be left floating. The external oscillator should operate between GND and the 1.8V VDD supply.

JTAG

JTAG_TCK (13) : JTAG TCK Input
JTAG_TDO (14) : JTAG TDO Output
JTAG_TMS (15) : JTAG TMS Input
JTAG_TDI (16) : JTAG TDI Input

Please refer to the *FE310-G003 Manual* for information on the JTAG and debug facilities.

QSPI

QSPI_DQ_3 (1) : Bidirectional Quad SPI Data Line
QSPI_DQ_2 (2) : Bidirectional Quad SPI Data Line
QSPI_DQ_1 (3) : Bidirectional Quad SPI Data Line
QSPI_DQ_0 (4) : Bidirectional Quad SPI Data Line
QSPI_CS (5) : Quad SPI Chip Select OUTPUT, Active Low.
QSPI_SCK (48) : Quad SPI Clock OUTPUT

Please refer to the *FE310-G003 Manual* for information on the SPI FLASH interface and to the Applications Notes and Errata section of this datasheet for information in the SPI implementation.

GPIO Multiplexed Outputs

The General Purpose Input/Output pins are multiplexed with PWM, SPI and UART functions as described in Table 2.1. GPIO pins may be configured as inputs or outputs, with a weak pull-up, and with two drive strengths. In addition, PWM, SPI and UART functions may be multiplexed on the pins through the GPIO control register. Please refer to the *FE310-G003 Manual* for information on GPIO capabilities.

Name	Pin	GPIO	PWM	SPI	UART	I2C
GPIO_0	25	0 I/O	PWM0_0 O			
GPIO_1	26	1 I/O	PWM0_1 O			
GPIO_2	27	2 I/O	PWM0_2 O	SPI1_SS0		
GPIO_3	28	3 I/O	PWM0_3 O	SPI1_MOSI		
GPIO_4	29	4 I/O		SPI1_MISO		
GPIO_5	31	5 I/O		SPI1_SCK		
GPIO_9	33	9 I/O		SPI1_SS2		
GPIO_10	34	10 I/O	PWM2_0 O	SPI1_SS3		
GPIO_11	35	11 I/O	PWM2_1 O			
GPIO_12	36	12 I/O	PWM2_2 O			I2C0 SDA
GPIO_13	37	13 I/O	PWM2_3 O			I2C0 SCL
GPIO_16	38	16 I/O			UART0_RX I	
GPIO_17	39	17 I/O			UART0_TX O	
GPIO_18	40	18 I/O			UART1_TX O	
GPIO_19	41	19 I/O	PWM1_1 O			
GPIO_20	42	20 I/O	PWM1_0 O			
GPIO_21	43	21 I/O	PWM1_2 O			
GPIO_22	44	22 I/O	PWM1_3 O			
GPIO_23	45	23 I/O			UART1_RX I	

Table 2.1: GPIO pin assignments.

AON Block Interface Pins

The following pins interface to the Always-ON (AON) block. AON Block I/O pins are 3.3V.

AON_PMU_OUT_0 (22) : Programmable SLEEP control OUTPUT.
AON_PMU_OUT_1 (17) : Programmable SLEEP control OUTPUT.
AON_PMU_DWAKEUP_N (18) : Digital Wake-From-Sleep INPUT, active LOW.
AON_ERST_N (24) : External System Reset INPUT, active LOW.
AON_PSD_LFALTCLK (20) : Optional 32kHz Clock Input.
AON_PS_LFCLKSEL (21) : 32kHz Clock Source Selector. When driven low, AON PSD LFALTCLK input is used as the 32 kHz low-frequency clock source. When left unconnected or driven high, the internal LFROSC source is used.

Chapter 3

Configuration and Block Diagram

Block Diagram

Figure 3.1 shows the overall block diagram of the FE310-G003 . The FE310-G003 contains an E31 Core Complex, a selection of flexible I/O peripherals, a dedicated off-chip Quad-SPI flash controller for execute-in-place, 8 KiB of in-circuit programmable OTP memory, clock generation, and an always-on (AON) block including a programmable power-management unit (PMU).

E31 Core Complex Configuration

The core is configured to support the RV32IMAC ISA options.

The branch predictor configuration has 48 branch-target buffer (BTB) entries, 128 branch-history (BHT) entries, and a two-entry return-address stack (RAS).

The integer multiplier completes 8 bits per cycle, so takes up to four clock cycles for a single 32×32 multiply operation.

The integer divider completes one bit per clock cycle, with an early out.

The instruction cache is a 16 KiB two-way set associative with 32-byte lines.

The data SRAM is 64 KiB.

CLINT

The Core Local Interrupt Controller (CLINT) supports the standard timer and software interrupts.

PLIC

The platform-level interrupt controller (PLIC) receives interrupt signals from the peripheral devices and prioritizes these for service by the core. The PLIC supports 7 programmable priority levels. Please refer to the chapter “FE310-G003 Interrupts” in the *SiFive FE310-G003 Manual* for more information on the PLIC implementation.

JTAG Connections

A four-wire 1149.1 JTAG connection is used to connect the external debugger to the internal debug module.

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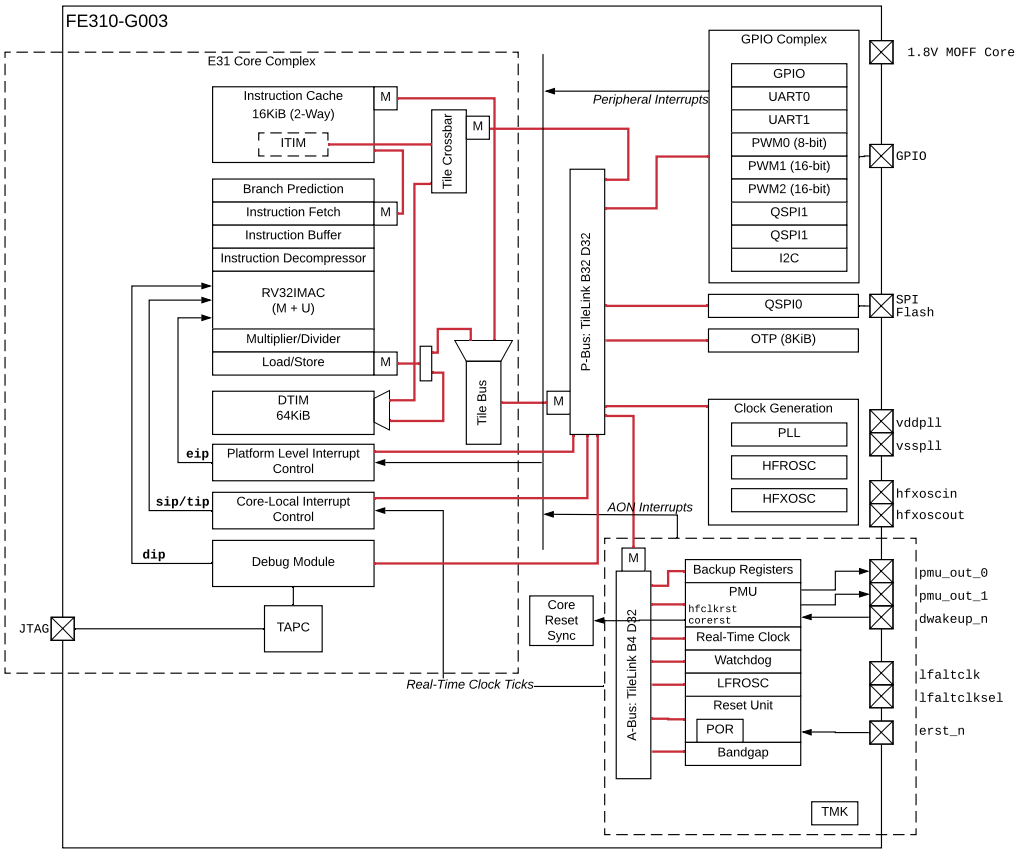

Figure 3.1: FE310-G003 top-level block diagram.

Debug Module

The debug module is accessed over JTAG, and has support for two programmable hardware breakpoints. The debug RAM has 28 bytes of storage.

Quad-SPI Flash

A dedicated quad-SPI (QSPI) flash interface is provided to hold code and data for the system. The QSPI interface supports burst reads of 32 bytes over TileLink to accelerate instruction cache refills. The QSPI can be programmed to support eXecute-In-Place modes to reduce SPI command overhead on instruction cache refills. The QSPI interface also supports single-word data reads over the primary TileLink interface, as well as programming operations using memory-mapped control registers.

GPIO Complex

The GPIO complex manages the connection of digital I/O pads to digital peripherals, including SPI, UART, and PWM controllers, as well as for regular programmed I/O operations. FE310-G003 has two additional QSPI controllers in the GPIO block, one with four chip selects and one with one.

FE310-G003 also has two UARTs and one I2C interface. FE310-G003 has three PWM controllers, two with 16-bit precision and one with 8-bit precision.

Always-On (AON) Block

The AON block contains the reset logic for the chip, an on-chip low-frequency oscillator, a watchdog timer, connections for an off-chip low-frequency clock source, the real-time clock, a programmable power-management unit, and 16×32-bit backup registers that retain state while the rest of the chip is powered down.

The AON can be instructed to put the system to sleep. The AON can be programmed to exit sleep mode on a real-time clock interrupt or when the external digital wakeup pin, `dwakeup_n`, is pulled low. The `dwakeup_n` input supports wired-OR connections of multiple wakeup sources.

Power Supply

FE310-G003 requires two dedicated power rails providing 1.8 V power to the core logic, and 3.3 V to the I/O pads and always on block.

Chapter 4

FE310-G003 Electrical Specifications

Note: Electrical specifications without MIN and/or MAX values are not thoroughly tested in production, and are provided for reference only. Except where otherwise noted, the typical electrical parameters are specified under the following conditions: Ambient Temperature 27C, VDD Supply Voltage 1.8V, IVDD Supply Voltage 3.3V, Processor Clock 16MHz crystal. ***These specifications are subject to change without notice.***

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IIVDD	IVDD Supply Current	ACTIVE, 16MHz		8		mA
		ACTIVE, 150MHz		13		mA
IVDD	VDD Supply Current	ACTIVE, 16MHz		8		mA
		ACTIVE, 150MHz		90		mA

Table 4.1: FE310-G003 Supply Voltage and Current Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIL	Input Voltage LOW Threshold	GPIO			0.8	V
VIH	Input Voltage HIGH Threshold	GPIO	2			V
VOL	Output Voltage LOW	GPIO, DS=0, 1mA DC Load		20		mV
		GPIO, DS=1, 1mA DC Load		16		mV
		GPIO, DS=1, 8mA DC Load		280	400	mV
		GPIO, DS=0, 20mA DC Load		380		mV
VOH	Output Voltage HIGH, with respect to VDDIO	GPIO, DS=0, 1mA DC Load		-18		mV
		GPIO, DS=1, 1mA DC Load		-14		mV
		GPIO, DS=1, 8mA DC Load	-900	-290		mV
		GPIO, DS=0, 20mA DC Load		-400		mV
IOL	Output Current LOW	GPIO, DS=0, VGPIO=0.3V		16		mA
		GPIO, DS=1, VGPIO=0.3V	11.5	21		mA
IOH	Output Current HIGH	GPIO, DS=0, VGPIO=3.0V		-15		mA
		GPIO, DS=1, VGPIO=3.0V	12.7	-21		mA
IPUL	Output Pull-Up Current (PUE=1)	GPIO, VGPIO=0V		-85		uA
		GPIO, VGPIO=2V		-75		uA
ILKH	Input Leakage, HIGH	GPIO, VGPIO=3.3V		200		pA
ILKL	Input Leakage, LOW	GPIO, VGPIO=0V		-100		pA
II	Input Leakage Current @ VI=3.3V or 0V	GPIO			$\pm$1	uA
IOZ	Tri-state Output Leakage Current @ VO=3.3V or 0V	GPIO			$\pm$1	uA

Table 4.2: FE310-G003 Input/Output Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FLFRO	Low Frequency Ring Oscillator Center Frequency		6	25	42	kHz
FHFRO	High Frequency Ring Oscillator Center Frequency		20	75	130	MHz
FMAX	Maximum Tested Operating Frequency			150		MHz

Table 4.3: FE310-G003 AC Characteristics

Chapter 5

FE310-G003 Application Notes and Errata

Boot Code

The FE310-G003 boots by jumping to the beginning of the OTP memory and executing code found there. Devices may be shipped with or without the OTP programmed, and pre-programmed OTP code will vary depending on the application.

Please refer to the OTP Application Notes section of this datasheet for more information on programming the OTP.

Chapter 6

FE310-G003 OTP Application Notes

OTP Programming Warnings

Warning: Improper use of the One Time Programmable (OTP) memory may result in a nonfunctional device and/or unreliable operation.

- OTP Memory must be programmed following the procedure outlined below *exactly*.
- OTP Memory is designed to be programmed or accessed only while the system clock is running between 1MHz and 37MHz.
- OTP Memory must be programmed **only** while the power supply voltages remain within specification.

OTP Programming Procedure

1. LOCK the otp:
   (a) Writing 0x1 to `otp_lock`
   (b) **Check that 0x1 is read back from** `otp_lock`.
   (c) Repeat this step until 0x1 is read successfully.
2. SET the programming voltages by writing the following values:

   ```
   otp_mrr=0x4
   otp_mpp=0x0
   otp_vppen=0x0
   ```

3. WAIT 20us for the programming voltages to stabilize
4. ADDRESS the memory by setting `otp_a`
5. WRITE **one bit at a time**:
   (a) set **only** the bit you want to write high in `otp_d`
   (b) Bring `otp_ck` HIGH for 50us

   (c) Bring `otp_ck` LOW.

   Note that this means **only** one bit of `otp_d` should be high at any time.

6. VERIFY the written bits setting `otp_mrr=0x9` for read margin.
7. SOAK any verification failures by repeating steps 2-5 using 400us pulses.
8. REVERIFY the rewritten bits setting `otp_mrr=0xF`. Steps `7,8` may be repeated up to 10 times before failing the part.
9. UNLOCK the otp by writing `0x0` to `otp_lock`.

Chapter 7

FE310-G003 Package Information

Package Outline Drawing - 48QFN

The FE310-G003 is offered in a convenient 48-lead 6x6 QFN package (0.4mm lead pitch). The exposed paddle (Pin 49) should be connected directly to the ground plane.

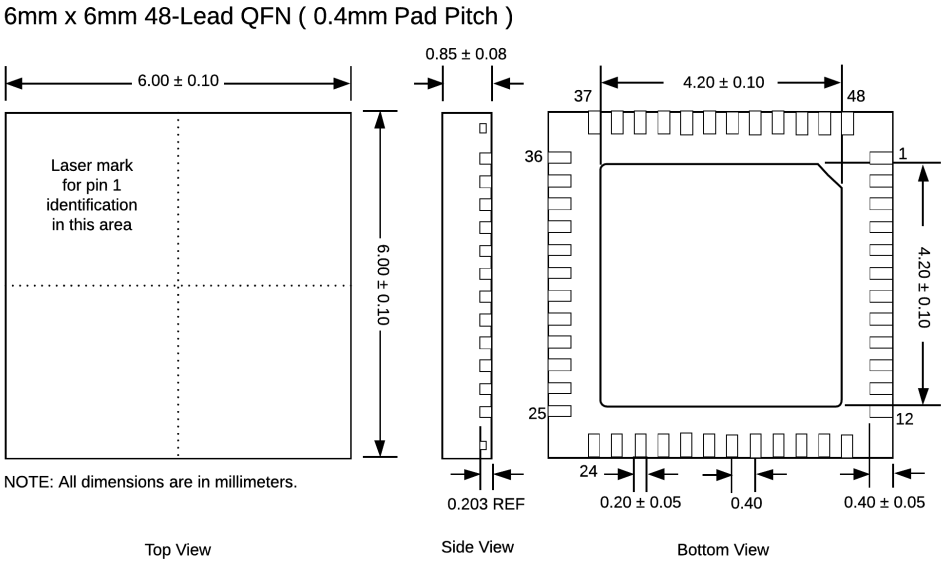

Figure 7.1: 48QFN Package Outline Drawing (0.4mm pitch)

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Recommended PCB Footprint - 48QFN

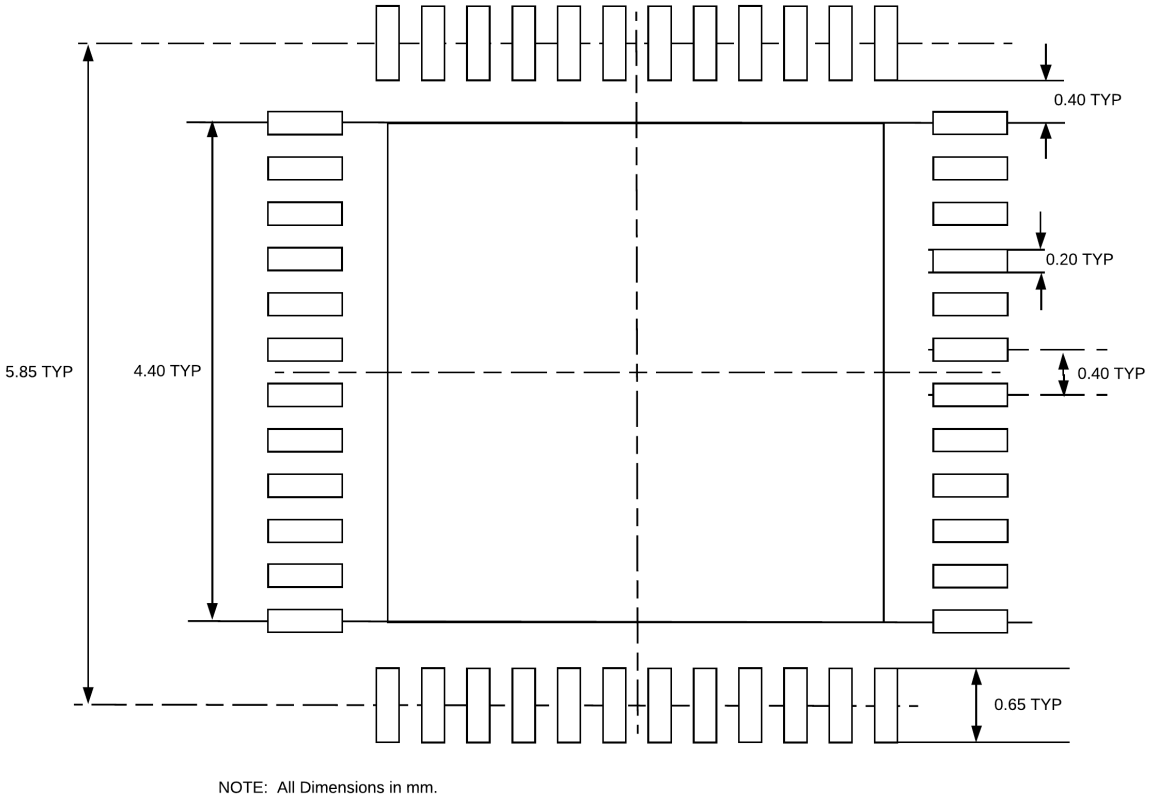

Figure 7.2: 48QFN PCB Footprint Drawing (0.4mm pitch)