# E85: Digital Design and Computer Engineering
## Problem Set 10

1) Modify the multicycle-cycle ARM processor to implement the BL instruction. Mark up copies of the controller, main decoder FSM, ALU decoder, and datapath (attached) to handle the new instruction as simply as possible. Name any control signals you need to add.

2) Goliath Corp claims to have a patent on a three-ported register file. Rather than fighting Goliath in Court, you offer to design a new register file with only two ports. Port 1 can be read or written, and port 2 is read-only. Redesign the multicycle datapath and controller (attached) to use your new register file.

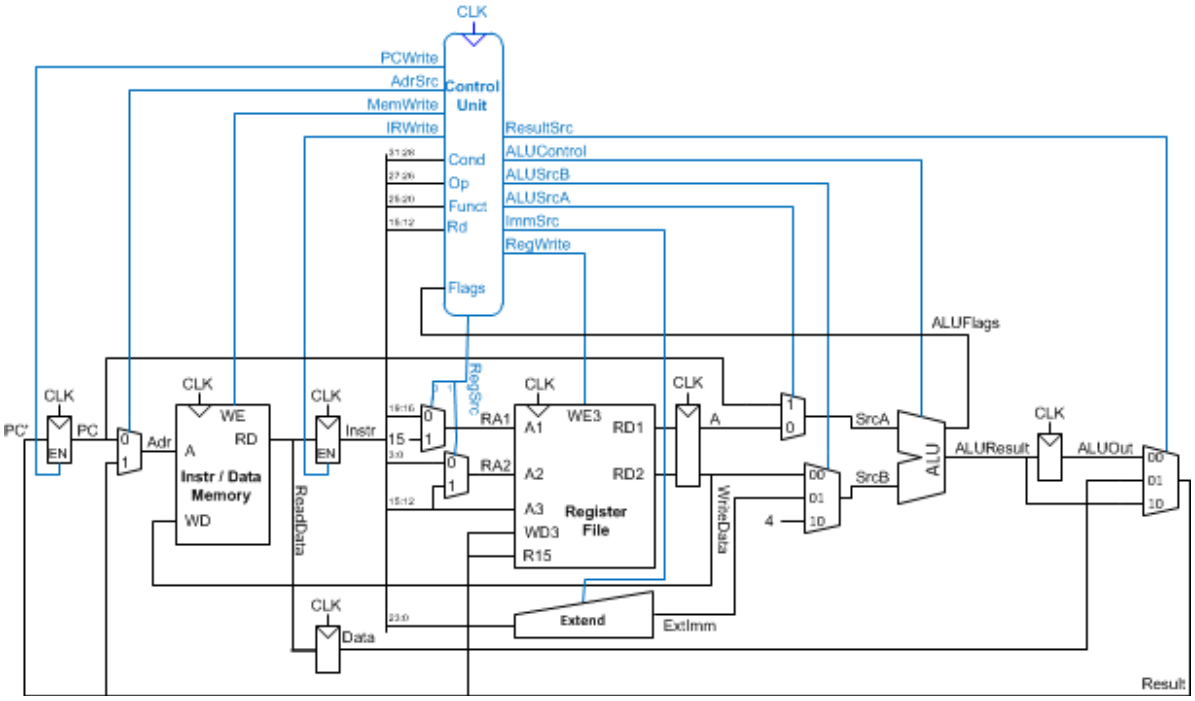
3) How long would your processor from the previous question take to execute the 10-billion instruction program from Example 7.6? Assume your new register file has 30% lower clk-to-Q and setup time because it has fewer ports but ordinary registers and other blocks have delay unchanged.

4) Do Exercise 7.28 from the textbook.

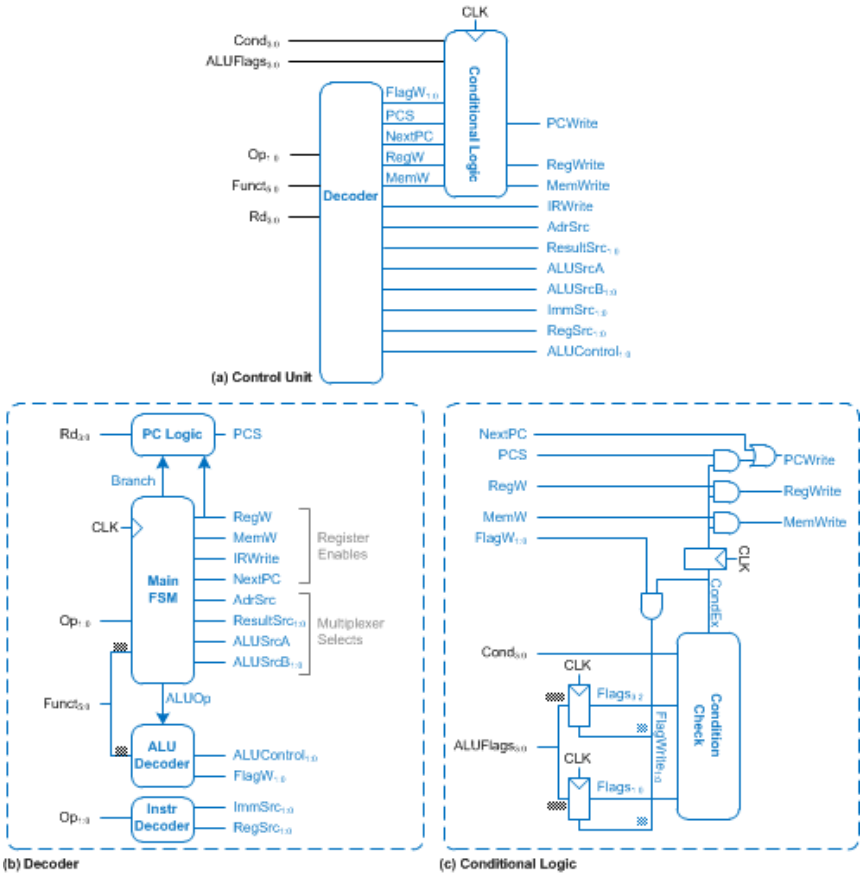
5) Do Exercise 7.30 from the textbook.

6) Impact on Society: Write a thoughtful paragraph describing a concrete example of how the skills you have developed in E85 may be applicable to another field of engineering in which you are interested in practicing.

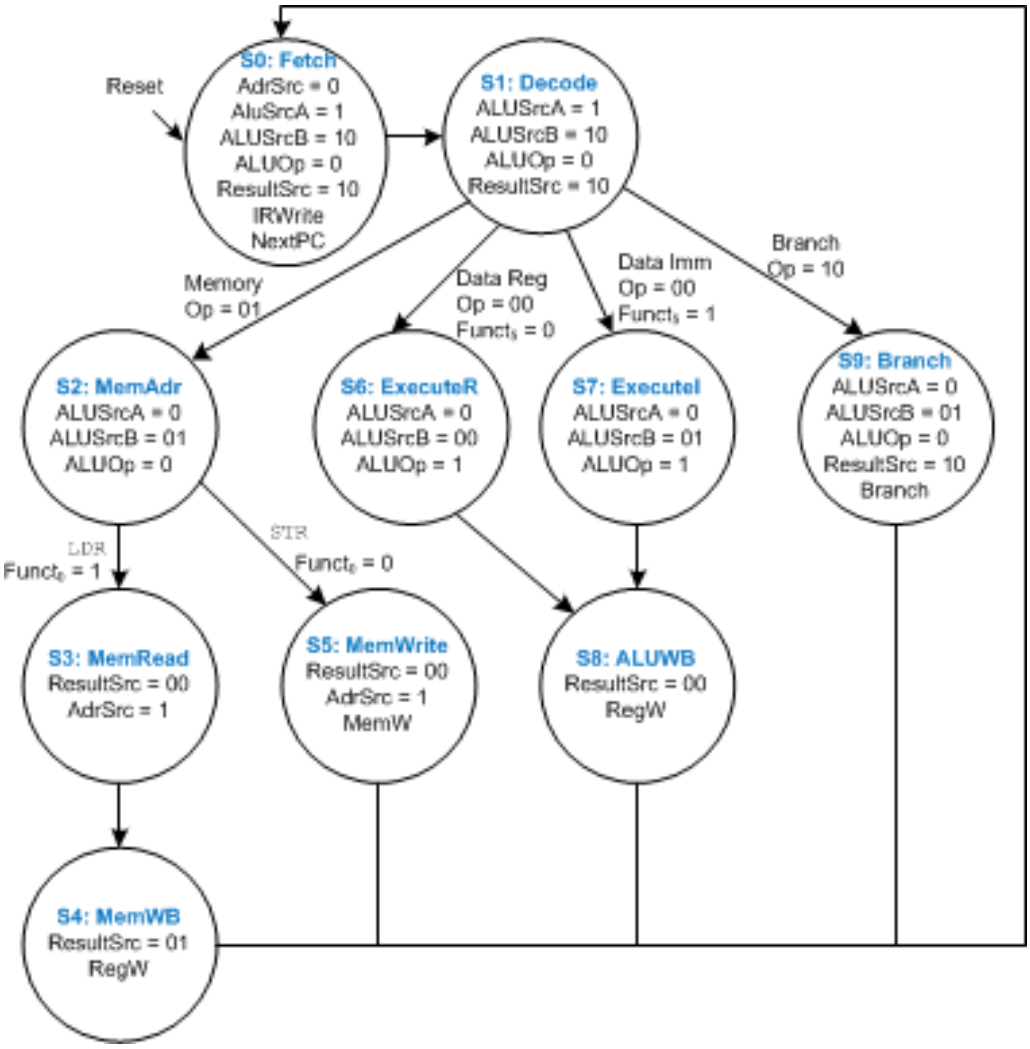
How long did you spend on this problem set? This will not count toward your grade but will help calibrate the workload.




Problem 2: Multicycle Datapath




Problem 2: Multicycle Controller

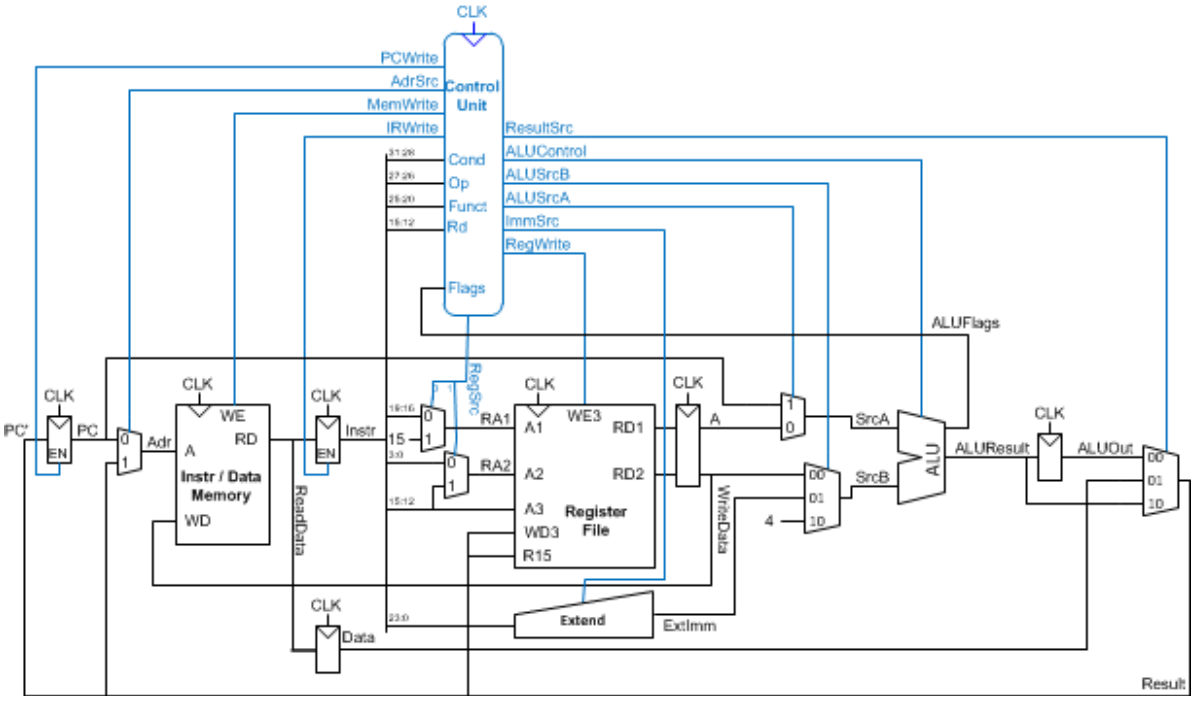



Problem 2: Multicycle Main Control FSM

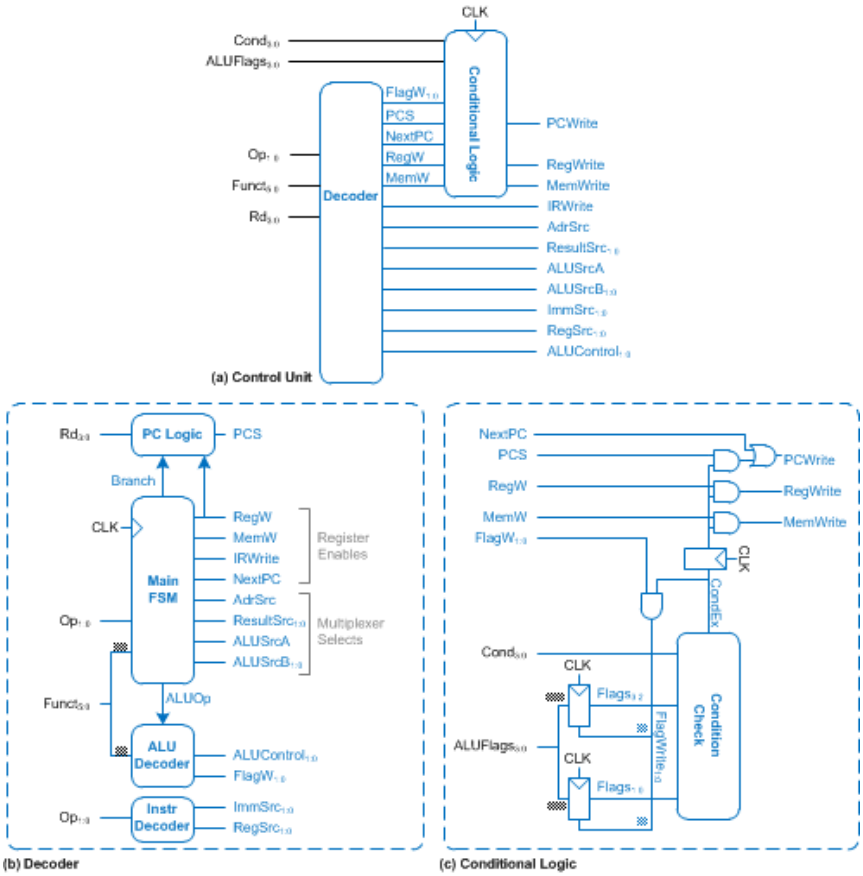
**Table 7.3 ALU Decoder truth table**

| *ALUOp* | $Funct_{4:1}$ (*cmd*) | $Funct_0$ (*S*) | Type | $ALUControl_{1:0}$ | $FlagW_{1:0}$ |
|---|---|---|---|---|---|
| 0 | X | X | Not DP | 00 (Add) | 00 |
| 1 | 0100 | 0 | ADD | 00 (Add) | 00 |
| | | 1 | | | 11 |
| | 0010 | 0 | SUB | 01 (Sub) | 00 |
| | | 1 | | | 11 |
| | 0000 | 0 | AND | 10 (And) | 00 |
| | | 1 | | | 10 |
| | 1100 | 0 | ORR | 11 (Or) | 00 |
| | | 1 | | | 10 |

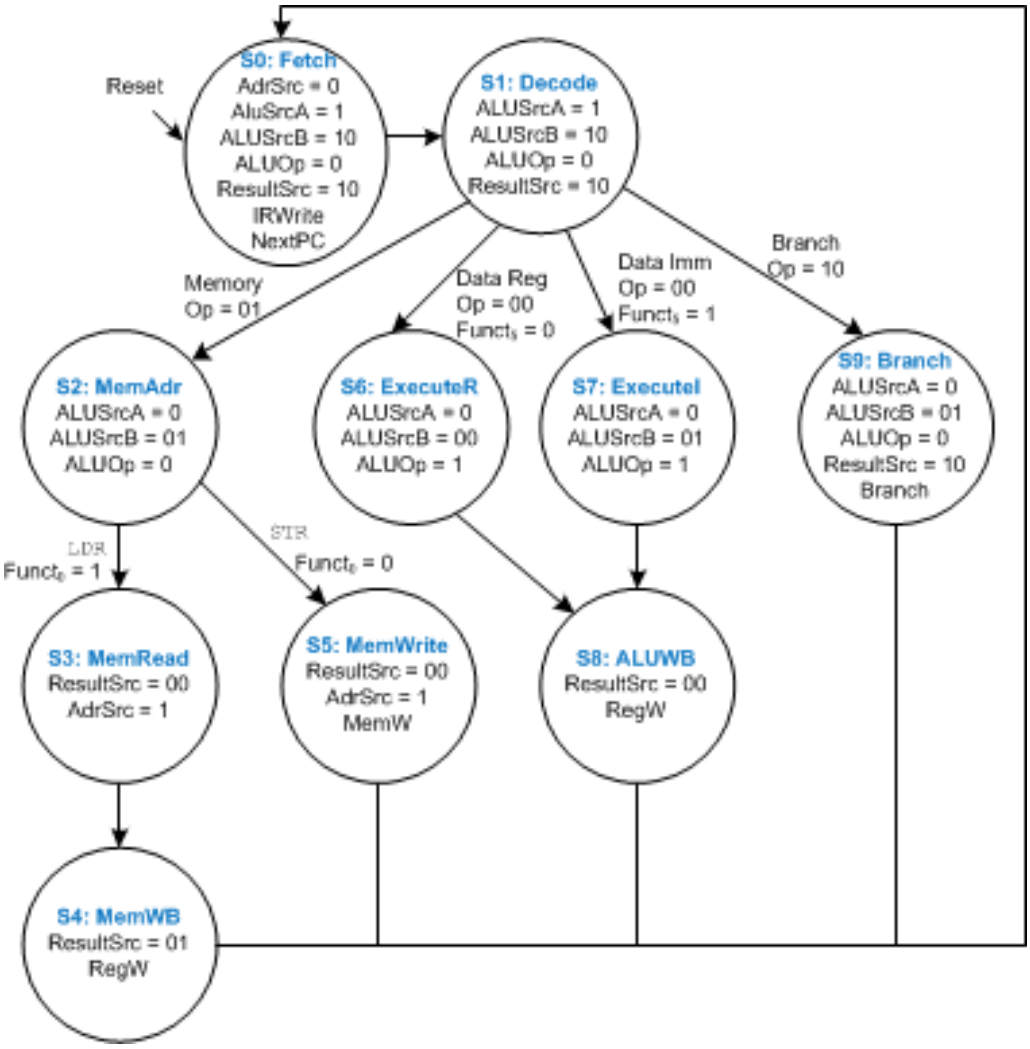
Problem 2: ALU Decoder




Problem 3: Multicycle Datapath




Problem 3: Multicycle Controller




Problem 3: Multicycle Main Control FSM

**Table 7.3 ALU Decoder truth table**

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| | 0010 | 0 | SUB | 01 (Sub) | 00 |
| | | 1 | | | 11 |
| | 0000 | 0 | AND | 10 (And) | 00 |
| | | 1 | | | 10 |
| | 1100 | 0 | ORR | 11 (Or) | 00 |
| | | 1 | | | 10 |

Problem 3: ALU Decoder