E85: Digital Design and Computer Engineering
Problem Set 5

1) SystemVerilog to State Transition Diagram

   Do Exercise 4.24 from the textbook.

2) SystemVerilog Logic Design

   Design a serial (one bit at a time) two's complementer FSM with two inputs, Start (same function as a Reset) and A, and one output, Q. Start is asserted to initialize the FSM before the least significant bit is provided. In other words, develop a machine that performs the two's complement operation on a binary number of arbitrary length, starting with the least significant bit. A one-bit input A simultaneously produces a one-bit output Q. For example, given 4'b0010, A receives '0' then '1', '0', '0', respectively and the FSM outputs '0', '1', '1', '1' with the corresponding output bit appearing at Q on the same cycle. Express your design in behavioral SystemVerilog.
   Hint: You may find it helpful to try some more cases by hand to figure out how the output should *depend* on the input. You may also want to look at Example 3.7 in Harris & Harris.

3) Priority Circuit

   An N-input lowest priority circuit has an N-bit input $A_{N-1:0}$ and an N-bit output $Y_{N-1:0}$. An output bit $Y_j = 1$ only if $A_k = 0$ for all $k < j$ and $A_j = 1$. Otherwise, $Y_j = 0$. In other words, it asserts a bit in Y corresponding to the *least* significant bit asserted in A.

   Design a 16-input lowest priority circuit with a propagation delay not exceeding 55 ps. Suppose each 2-input gate has a delay of 10 ps and an inverter has a delay of 5 ps. Sketch a schematic for your circuit. If you are spending too much time on this problem, you may relax the delay requirement to 180 ps for partial credit.

   Hint: You may want to start from a 2-input priority circuit. How would you design it? Then, increase the input size and look for any pattern. Think about how to generalize the pattern so your design is neat and easy to draw.

4) Impact on Society: Identify a product that you use directly or indirectly in your life that contains an FPGA. Why would the designers choose to use an FPGA in that product?

5) AI Question (Optional)
   This question must be solved by AI. Report what the AI produces, whether you believe it is accurate or a hallucination, and whether the solution is similar, better, or worse than what you would have done yourself in a reasonable amount of time.

   Design a finite state machine in SystemVerilog to determine if a binary number is divisible by 3. The number arrives bit-serially, with the least significant bit first.

How long did you spend on this problem set? This will not count toward your grade but will help calibrate the workload.