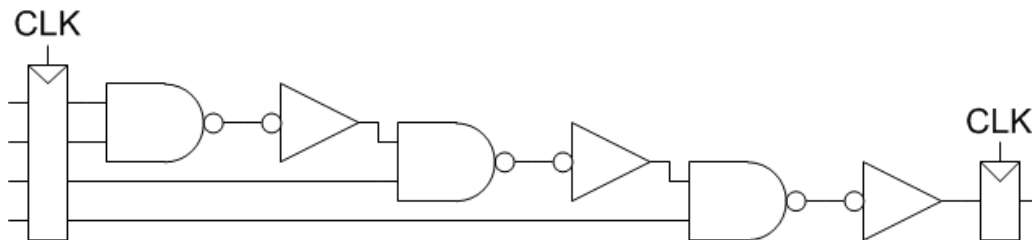# E85: Digital Design and Computer Engineering
Problem Set 4

1) Reconsider the circuit from PS3, with registers added. What is the minimum clock period for the circuit in the absence of clock skew? How much clock skew could the circuit endure before possibly violating the hold time?

Cell	Propagation Delay (ps)	Contamination Delay (ps)	Setup Time (ps)	Hold Time (ps)
NOT	6	4		
NAND (2-input)	8	6		
NOR (2-input)	10	8		
NAND (3-input)	10	8		
NOR (3-input)	12	10		
Flop	20	15	10	5

2) Synchronizers

Do Exercise 3.36 from the textbook.

3) SystemVerilog

Do Exercises 4.2 and 4.13 from the textbook. Use behavioral Verilog for 4.13.

4) Impact on Society: What mean time between failure would you target for a synchronizer in a life-critical medical device? Justify your choice. If the only synchronizer element readily available to you has a MTBF of 10^9 seconds, how could you achieve your target?

5) AI Question (Optional)
   This question must be solved by AI. Report what the AI produces, whether you believe it is accurate or a hallucination, and whether the solution is similar, better, or worse than what you would have done yourself in a reasonable amount of time.

   Write a SystemVerilog module for an 8-input priority encoder with input A[7:0] and output Y[2:0].

How long did you spend on this problem set? This will not count toward your grade but will help calibrate the workload.