

Digital Electronics & Computer Engineering (E85)

Harris & Chang

Fall 2019

Midterm



This is a closed-book take-home exam. Electronic devices including calculators are not allowed. You are permitted one side of one 8.5x11" sheet of paper with notes.

You are bound by the HMC Honor Code while taking this exam.

This is a 75-minute exam. You are responsible for monitoring your time.

Return the exam under Prof. Harris' door no later than Wednesday 10/16 at 9:30 am.

Along side each question, the number of points is written in brackets. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Show your work for partial credit.

Name: _____

Score

Page 2:	_____	/ 6
Page 3:	_____	/ 5
Page 4:	_____	/ 8
Page 5:	_____	/ 6
Total:	_____	/ 25

Determine the decimal value of 10010_2 interpreted as:

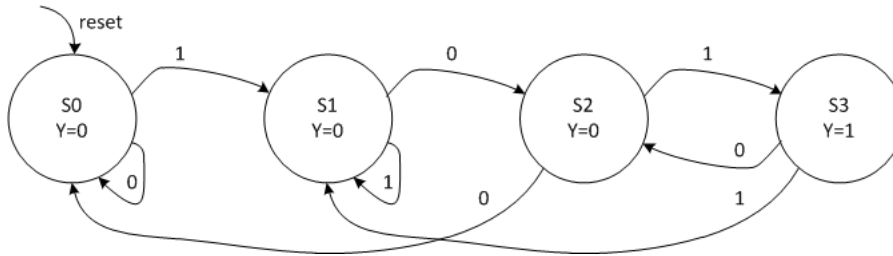
An unsigned binary number: _____ [1]

A two's complement binary number: _____ [1]

A sign/magnitude binary number: _____ [1]

[3] Sketch a CMOS transistor-level implementation of an OR-AND-INVERT (OAI) gate that computes $Y = \sim((A + B)C)$. Build it as a single gate, not a cascade of multiple gates. Use as few transistors as possible.

Consider the following Finite State Machine:



[2] Suppose that after the system is reset, the input sequence is 11010100100101011. On how many cycles will the output Y be 1?

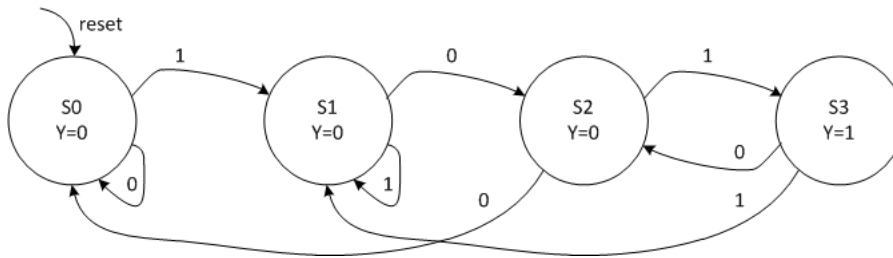
[3] Write a succinct behavioral SystemVerilog description of the FSM.

```
module fsm(input logic clk, reset,  
           input logic a,  
           output logic y);
```

```
    typedef enum logic [1:0] {S0, S1, S2, S3} statetype;  
    statetype state, nextstate;
```

```
endmodule
```

Consider the same finite state machine, repeated here for your convenience.



[3] Assuming a two-bit state encoding ($S_{1:0}$) of $S_0=00$, $S_1=01$, $S_2=10$, and $S_3=11$, write the next state and output tables for the FSM.

State		Input	Next State	
S_1	S_0	A	S_1'	S_0'
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

State		Output
S_1	S_0	Y
0	0	
0	1	
1	0	
1	1	

[3] Write Boolean equations for the next state and output.

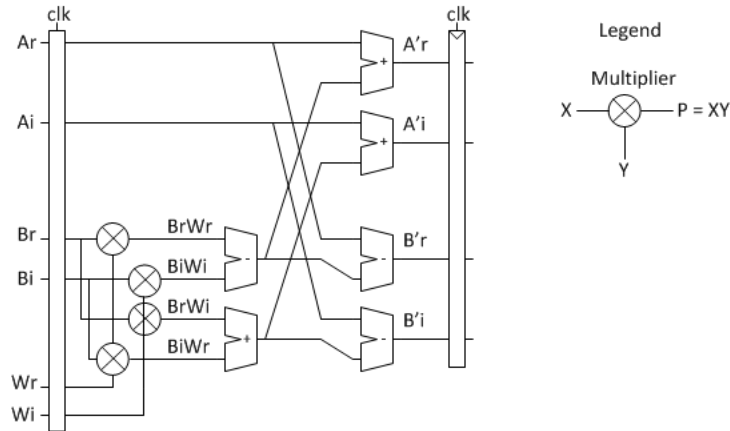
$$S_1' =$$

$$S_0' =$$

$$Y =$$

[2] Sketch the circuit.

The following circuit is the Butterfly Unit for a Radix-2 Fast Fourier Transform (FFT) unit. The Butterfly Unit receives complex inputs A and B, each of which have a real (r) and imaginary (i) part, and computes complex outputs $A' = A + B \cdot W$ and $B' = A - B \cdot W$. The circuit is built from real multipliers, adders, and subtractors.



Suppose the propagation and contamination delays of a multiplier are 250 and 20 ps, respectively, and the propagation and contamination delays of an adder or subtractor are 100 and 15 ps. The registers have propagation and contamination delays of 27 and 22 ps, a setup time of 23 ps, and a hold time of 11 ps.

[3] If there is no clock skew, find the minimum clock period of the circuit.

[3] If the clock period is long, how much clock skew can the system tolerate reliably?