

Digital Design & Computer Architecture (E85)

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Fall 2007

Final Exam

This is a closed-book take-home exam. You are permitted a calculator and two 8.5x11" sheets of paper with notes. The exam is due at Prof. Harris' office no later than noon on Tuesday December 18. You may spend no more than 5 hours on the exam, and once you start work, you may not discuss the exam with anybody else or consult any references or use a computer. Remember that the Harvey Mudd College Honor Code applies.

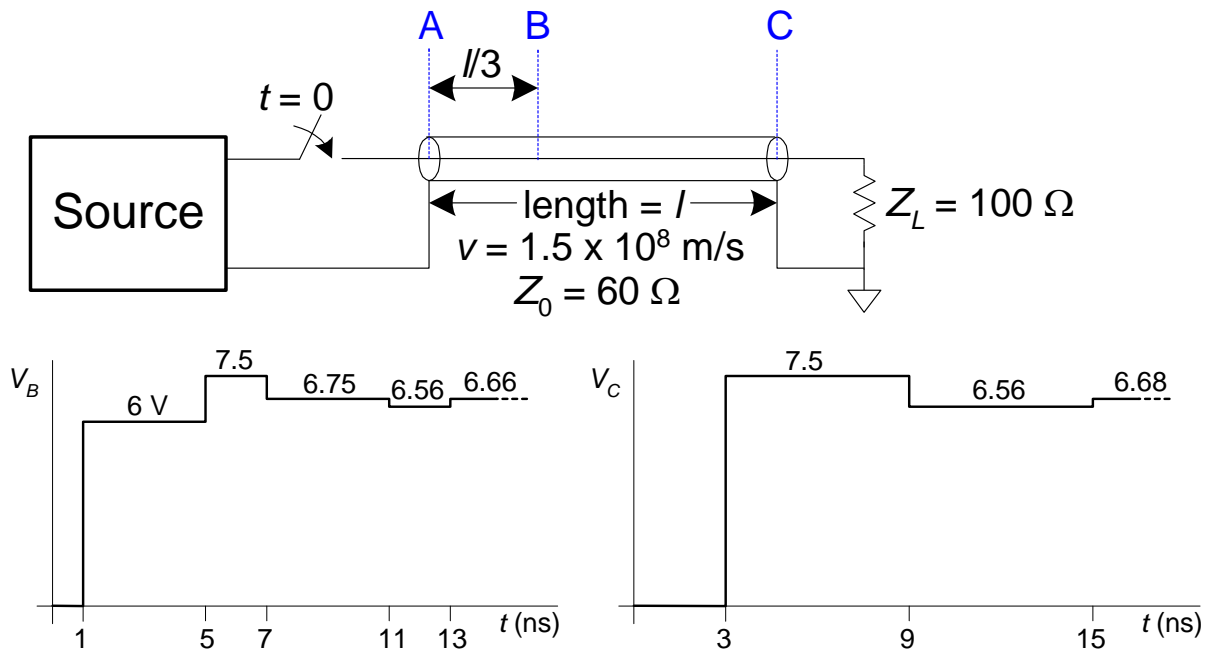
Along side each question, the number of points is written in brackets. The entire exam is worth 50 points. Plan your time accordingly. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Write neatly; illegible answers will be marked wrong. Show your work for partial credit.

Name: _____

Do Not Write Below This Point

Page 2:	_____	/6
Page 3:	_____	/8
Page 4-6:	_____	/6
Page 7-9:	_____	/15
Page 10:	_____	/4
Page 11-12:	_____	/11
Total:	_____	/50

1. The voltages at points B and C along a transmission line are shown below. The receiver has a $100\ \Omega$ input impedance, but the driver (source) is unknown.



(a) [2] If the speed of light in the transmission line is $1.5 \times 10^8\ \text{m/s}$, what is the length of the transmission line?

Length: _____

(b) [4] Draw a picture of the driver (source) of the circuit. Label the source voltage and source impedance.

2. You are given the following MIPS assembly code for a procedure called `proc1`.

```
proc1:
    add  $s1, $0, $0
    add  $v0, $0, $0
count: beq  $a0, $0, done
    andi $t0, $a0, 0x1
    beq  $t0, $0, shift
    addi $s1, $s1, 1
shift: srl  $a0, $a0, 1
    jal  proc1
done:  add  $v0, $v0, $s1
    jr   $ra
```

(a) [2] Suppose `proc1` is called with `0x1248421F` in `$a0`. Will the `proc1` function successfully return to the caller? Explain.

(b) [3] The procedure is missing some saving and restoring of variables. Add the minimum amount of code necessary to make the procedure operate correctly. Mark your changes in the code above by drawing arrow(s) where new code needs to be added and writing the new code nearby.

(c) [3] What value is returned by the corrected procedure in `$v0` when `$0x1248421F` is passed in `$a0`?

Return value: _____

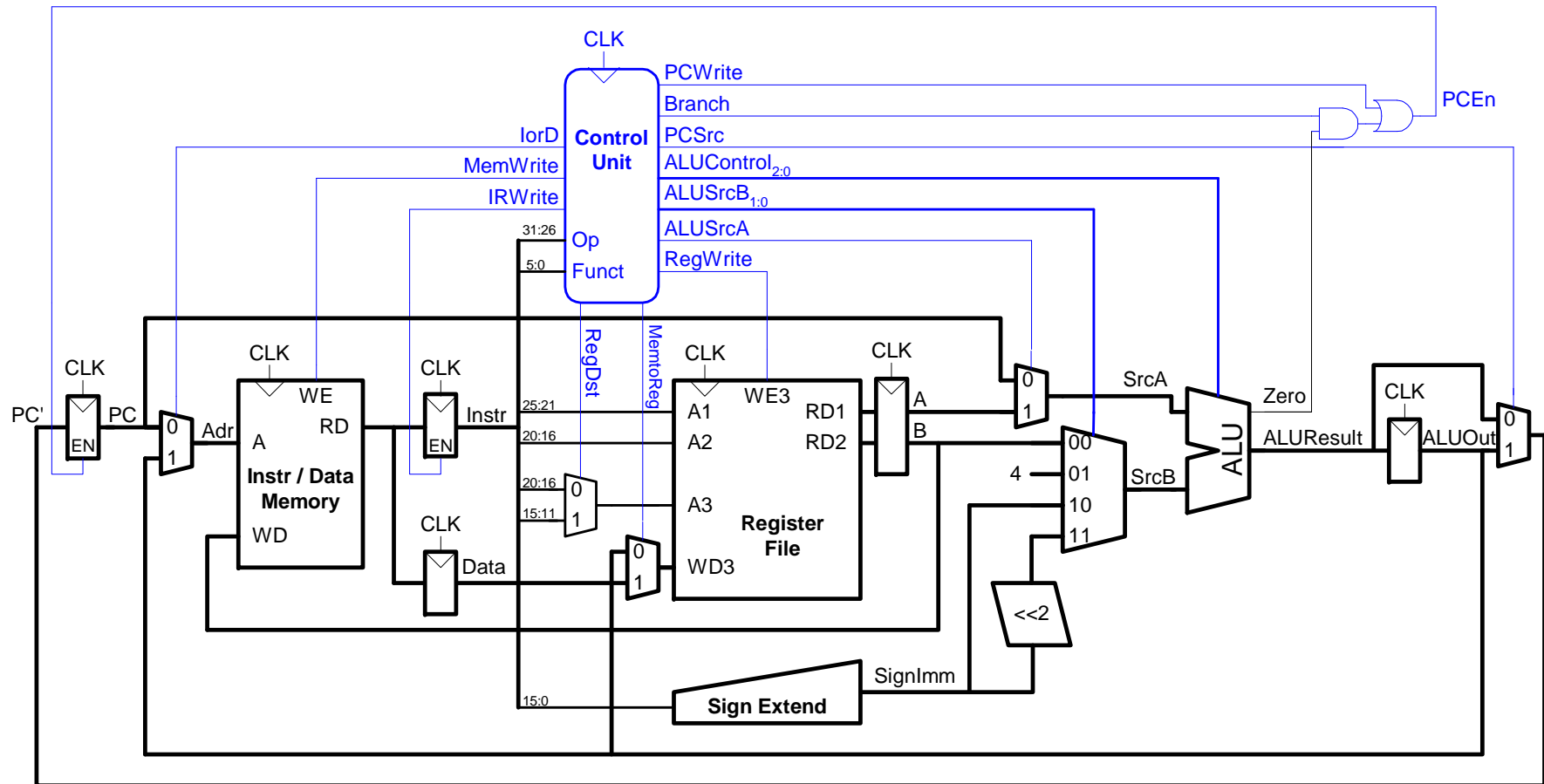
3 [6] Modify the MIPS multicycle processor to implement the `blez` instruction. On a `blez` instruction, the processor should branch to the branch target address (BTA) when the specified register is less than or equal to zero. An example of the `blez` instruction is:

Assembly: `blez $t0 loop`

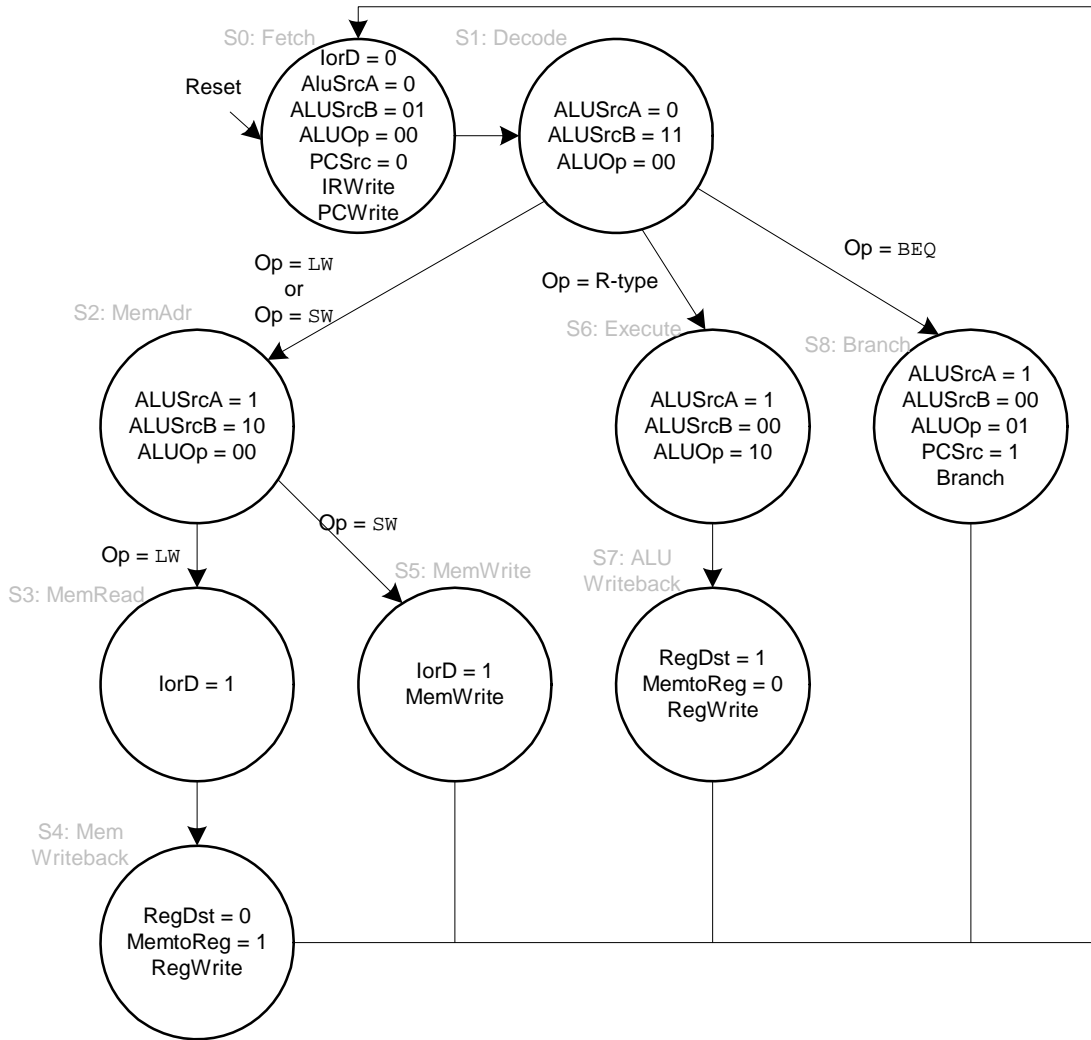
Machine code fields:

0x6	0x8	0x0	imm
opcode	rs	rt	imm

The original MIPS multicycle processor schematic and control finite state machine are given in the figures on the next two pages for your convenience. If you add any control signals, clearly label them. If you add any new functional blocks, clearly define what they do.



MIPS multicyle processor schematic



MIPS multicycle processor control finite state machine

4. You are given the Verilog code of the mystery module below.

```
module mystery(input  clk, a, b, reset,
               output q);
  wire [3:0] n, p;
  wire y1, y2, y3, y4, y5, y6;

  reg_r reg1(clk, reset, n[3], p[3]);
  reg_r reg2(clk, reset, n[2], p[2]);
  reg_s reg3(clk, reset, n[0], p[0]);
  reg_r reg4(clk, reset, (p[0]&a)&(b | a~b), p[1]);

  and2 and2_1(p[1], a, y1);
  and2 and2_2(p[2], a, y2);
  or2  or2_1(y1, y2, n[2]);

  and2 and2_3(p[0], ~a, y3);
  and2 and2_4(p[2], ~a, y4);
  and2 and2_5(p[1], ~a, y5);
  or2  or2_2(y3, y4, y6);
  or2  or2_3(y5, y6, n[0]);

  and2 and2_6(~p[1], ~p[0], q);
endmodule

module reg_r (input      clk, reset, a,
              output reg q);
  always @(posedge clk, posedge reset)
    if (reset) q <= 1'b0;
    else q <= a;
endmodule

module reg_s (input      clk, set, a,
              output reg q);
  always @(posedge clk, posedge set)
    if (set) q <= 1'b1;
    else q <= a;
endmodule

module and2 (input  a, b,
             output y);
  assign y = a & b;
endmodule

module or2 (input  a, b,
            output y);
  assign y = a | b;
endmodule
```

(a) [3] Sketch the circuit literally implied by the Verilog module. It should involve only flip-flops, 2-input AND and OR gates, and inverters. Do not perform any logic optimization.

(b) [3] Suppose each 2-input gate in part (a) has a propagation delay of 270 ps and contamination delay of 225 ps. Each inverter has a propagation delay of 100 ps and contamination delay of 87 ps. Each flip-flop has a propagation delay of 50 ps, a contamination delay of 20 ps, and setup and hold times of 40 ps and -10 ps, respectively. Assume that inputs a and b come directly from flip-flops in another module. What is the fastest clock speed that your circuit from part (a) can run at reliably?

Fastest Clock Speed: _____ (MHz)

(c) [3] If the clock period can be increased to be arbitrarily long, how much clock skew can the system withstand before it no longer works reliably?

Maximum Clock Skew: _____ (ps)

(d) [2] Describe clearly and concisely in words what the `mystery` circuit does.

(e) [4] Simplify the circuit from part (a) as much as possible and write Verilog code to represent your new circuit.

```
module mystery(input  clk, a, b, reset,  
               output q);
```

```
endmodule
```

5. Use MIPS memory-mapped I/O to interact with a user. Whenever the user holds down a button, 0x15 displays on 5 light emitting diodes (LEDs). Otherwise, the LEDs are OFF. Suppose the input button is mapped to address 0xFFFFF10 and the LEDs are mapped to address 0xFFFFF14. When the button is pushed, its output is 1; otherwise it is 0.

[4] Write MIPS code to implement this functionality. Comment your code.

6. Short Answer Questions

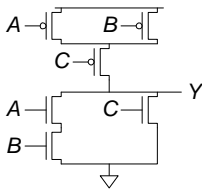
(a) [3] Consider a 32-word 2-way set associative cache with a block size of 4 words. A program repeatedly loads words from the following sequence of addresses:

24 28 2C 30 38 60 64 80 84 AC

Assuming least-recently used (LRU) replacement and ignoring startup effects (compulsory misses), what is the miss rate of the cache?

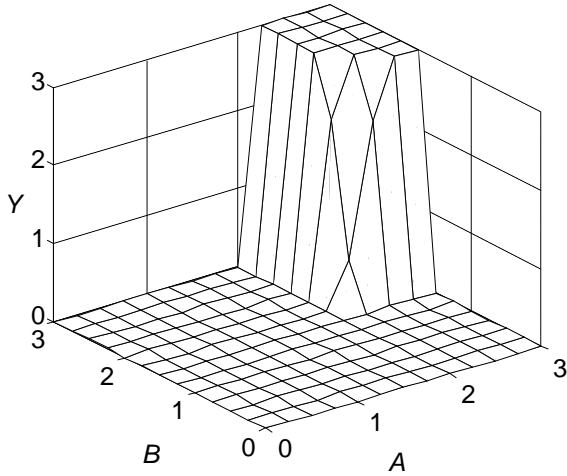
Miss Rate: _____

(b) [2] Write a Boolean equation for the function performed by the circuit shown below.



Equation: _____

(c) [3] A circuit has two inputs, A and B, and an output Y. The transfer characteristics are plotted below. Choose logic levels such that the circuit performs a Boolean function and name the function.



V_{IL}: _____
V_{IH}: _____
V_{OL}: _____
V_{OH}: _____
Function: _____

(d) [3] A pipelined MIPS processor is running the following program. Which registers are being read and which is being written on the fifth cycle?

```
add $s0, $t0, $t1
sub $s1, $t2, $t3
and $s2, $s0, $s1
or  $s3, $t4, $t5
slt $s4, $s2, $s3
```

Registers read: _____
Registers written: _____