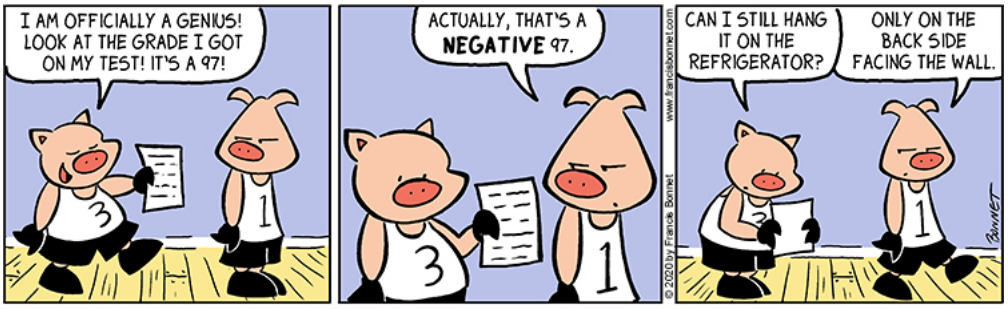
Digital Electronics & Computer Engineering (E85)

Harris Spring 2023

Midterm



This is a closed-book take-home exam. Electronic devices including calculators are not allowed. You are permitted one side of one 8.5 × 11" sheet of paper with notes.

You are bound by the HMC Honor Code while taking this exam.

This exam is intended to be doable in 75 minutes if you have prepared well. However, it has no time limit. You must complete the exam in one contiguous sitting without interruptions (e.g. meals, naps, conversations with other people; bathroom breaks are permitted).

Return the exam to Prof. Harris' office by March 3 at 5 pm.

Alongside each question, the number of points is written in brackets. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Show your work for partial credit.

Name: _____

Score

Page 3:	_____	/ 6
Page 4:	_____	/ 4
Page 5:	_____	/ 6
Page 6:	_____	/ 8
Page 7:	_____	/ 3
Total:	_____	**/ 27**

Reference

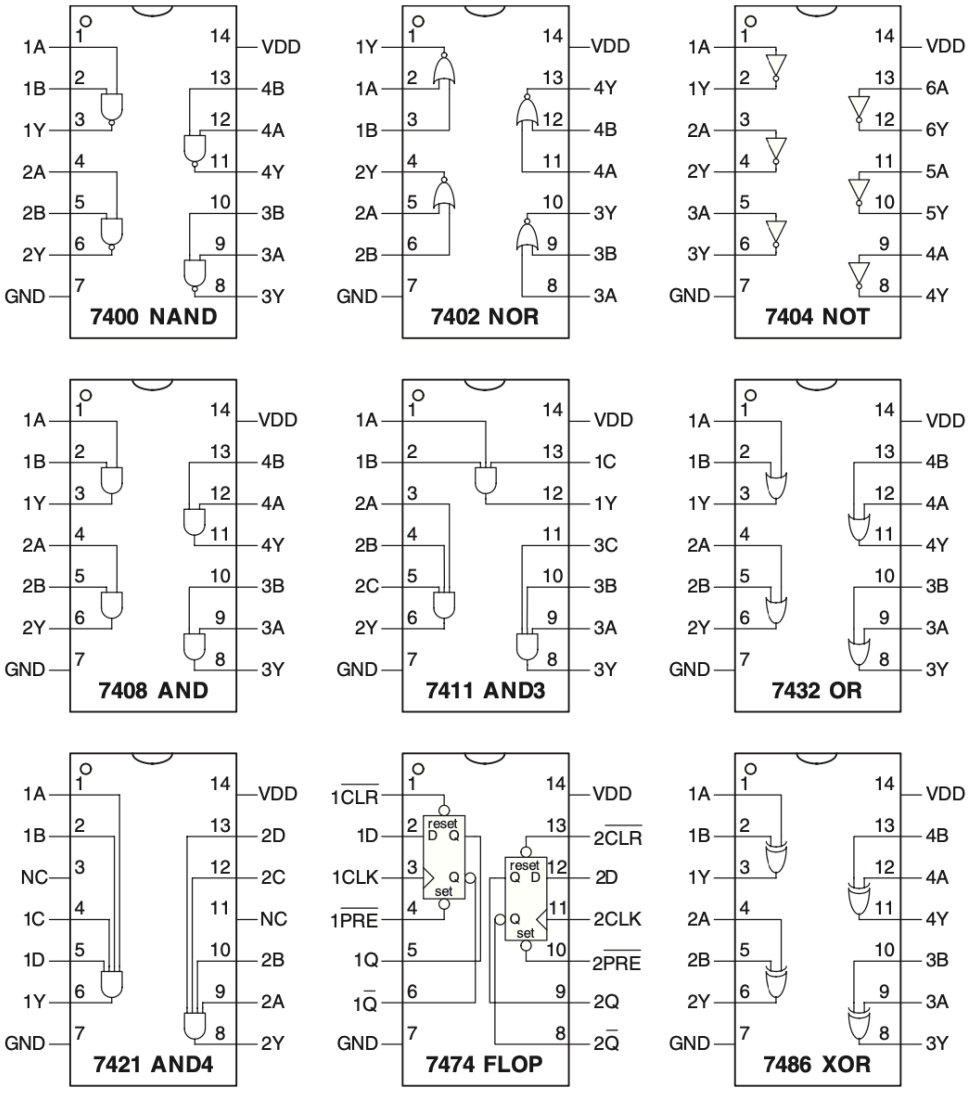
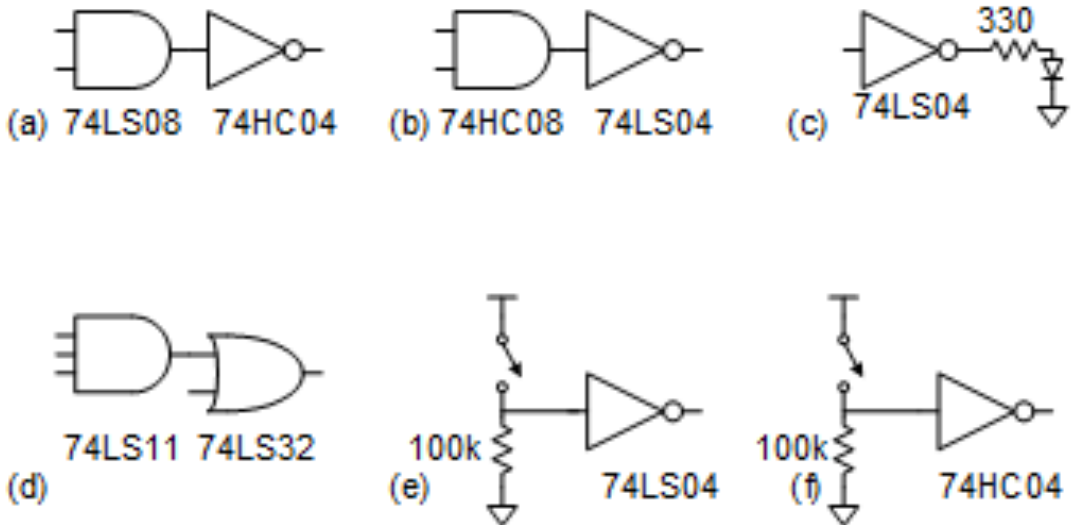


Figure eA.1 Common 74xx-series logic gates

Table eA.2 Typical specifications for 5-V logic families

Characteristic	Bipolar/TTL						CMOS		CMOS/TTL Compatible	
	TTL	S	LS	AS	ALS	F	HC	AHC	HCT	AHCT
t_{pd} (ns)	22	9	12	7.5	10	6	21	7.5	30	7.7
V_{IH} (V)	2	2	2	2	2	2	3.15	3.15	2	2
V_{IL} (V)	0.8	0.8	0.8	0.8	0.8	0.8	1.35	1.35	0.8	0.8
V_{OH} (V)	2.4	2.7	2.7	2.5	2.5	2.5	3.84	3.8	3.84	3.8
V_{OL} (V)	0.4	0.5	0.5	0.5	0.5	0.5	0.33	0.44	0.33	0.44
I_{OH} (mA)	0.4	1	0.4	2	0.4	1	4	8	4	8
I_{OL} (mA)	16	20	8	20	8	20	4	8	4	8
I_{IL} (mA)	1.6	2	0.4	0.5	0.1	0.6	0.001	0.001	0.001	0.001
I_{IH} (mA)	0.04	0.05	0.02	0.02	0.02	0.02	0.001	0.001	0.001	0.001
I_{DD} (mA)	33	54	6.6	26	4.2	15	0.02	0.02	0.02	0.02
C_{Pd} (pF)	n/a						20	12	20	14
cost* (US $)	obsolete	0.63	0.25	0.53	0.32	0.22	0.12	0.12	0.12	0.12

[6] Consider the logic gates and families on page 2. For example, recall that a 74LS08 is a 2-input AND gate with properties from the LS family. If the input or output is not shown, assume it is satisfactory for the application. For each of the following circuits, mark that it works reliably within the typical specifications, or explain what specification is violated.



(a) Works / Violates _____

(b) Works / Violates _____

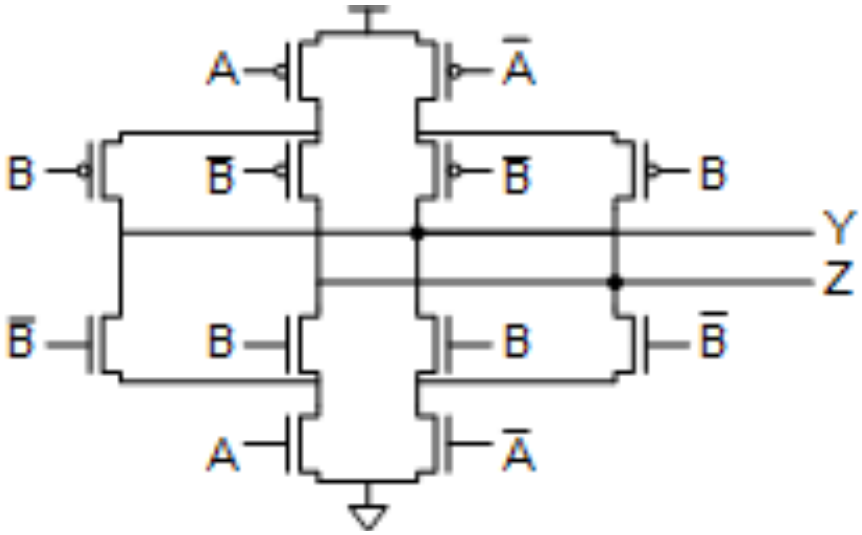
(c) Works / Violates _____

(d) Works / Violates _____

(e) Works / Violates _____

(f) Works / Violates _____

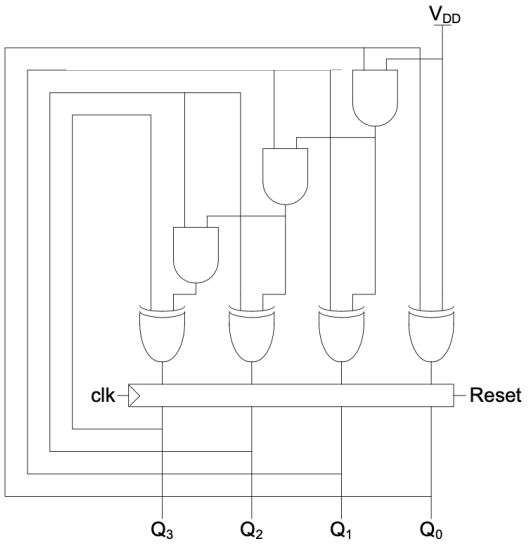
[4] Write Boolean equations for Y and for Z in terms of A and B.



Y = _____

Z = _____

Your firm, Spaced Out Circuits, designs digital systems for interplanetary missions. The previous engineer on the job spent three months designing the following circuit before being fired. Your boss says that it doesn't run fast enough, costs too much to produce, and that the engineer left no documentation of what it is supposed to do.



The space-qualified digital components available to you have the following specs:

Component	Unit cost	Propagation Delay (ps)	Contamination Delay (ps)
Inverter	$3	20	15
Buffer	$4	30	25
AND2 / OR2	$15	35	25
AND3 / OR3 / XOR2	$20	40	30
Resettable Flip-Flop	$30	32	15

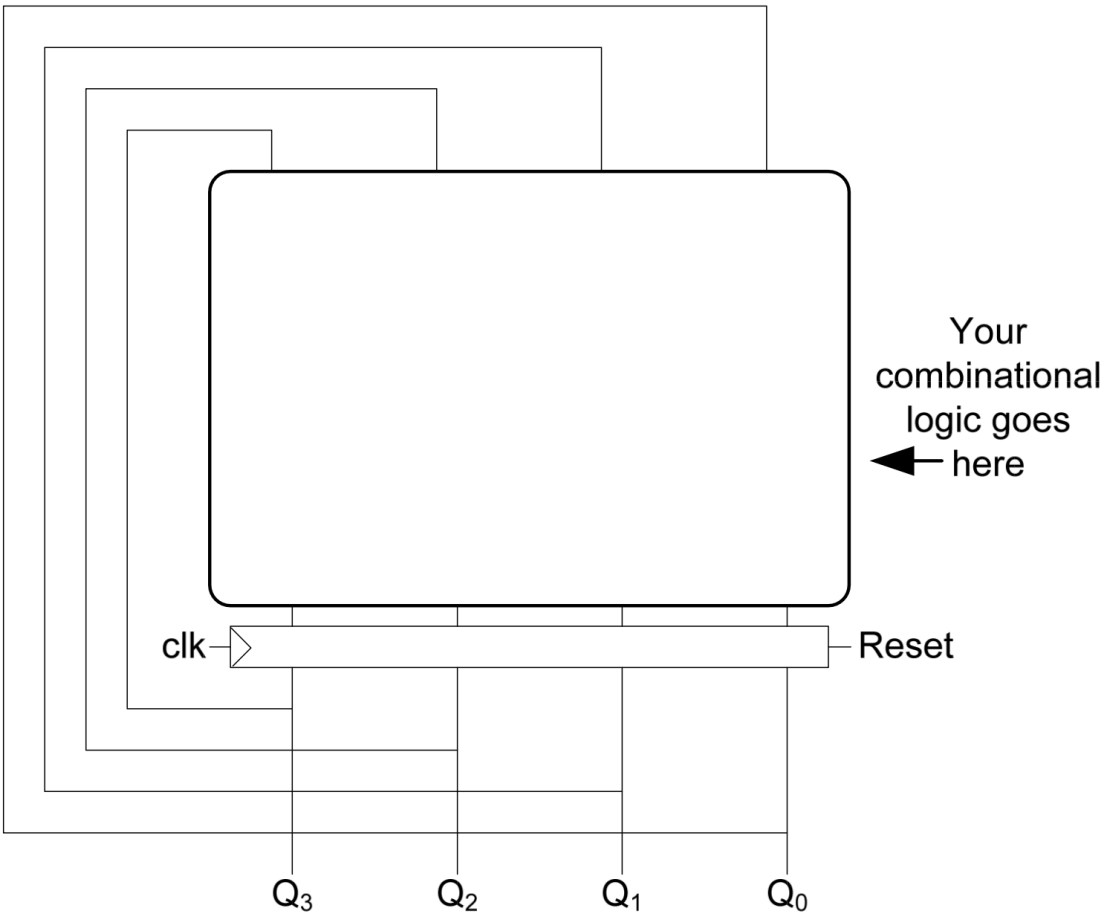
The flip-flop also has a setup time of 22 ps and a hold time of 28 ps. The current design costs $\$30 \times 4 + \$20 \times 4 + \$15 \times 3 = \$245$.

[2] Describe what the circuit does as clearly and concisely as possible.

[2] What is the minimum clock period at which the circuit will operate correctly if there is no skew?

[2] How much clock skew can the circuit withstand and still operate correctly if the clock period is 500 ps?

[5] Suppose the actual clock skew may be up to 20 ps. Redesign the combinational logic to run as fast as possible. Choose the lowest-cost solution that achieves this speed and works reliably. Sketch your design in the box below.



[2] What is the clock period at which your improved circuit will operate correctly if the clock skew may be up to 20 ps?

[1] What is the cost of your improved circuit?

[3] Write the shortest and simplest Verilog code that you can to describe the circuit.

```
module mystery(input  logic       clk, reset,
               output logic [3:0] Q);









endmodule
```