Project Rubric

Designers:
Chip:

Proposal:	**___ / 10**
Unambiguous, measurable functional description	___ / 4
Appropriate scope	___ / 2
Complete pinout with 2-phase clocking	___ / 1
Floorplan with credible justification	___ / 3
Verilog	**___ / 15**
Test bench demonstrates functions specified in proposal	___ / 5
Passes self-checking test bench	___ / 5
Suitable for conversion to schematics	___ / 3
Readable / commented	___ / 2
Schematic	**___ / 10**
At least one custom leaf cell	___ / 2
At least one custom block	___ / 3
At least one synthesized block	___ / 1
Pad frame	___ / 1
Passes self-checking test-bench	___ / 3
Analog blocks simulate in SPICE (if applicable)	___ / + 1
Block Layout	**___ / 5**
Leaf cell drawn cleanly	___ / 1
Synthesized block layout	___ / 1
Custom block > 50% complete & clean	___ / 1
DRC	___ / 1
LVS	___ / 1
Final Project	**___ / 30**
Layout complete, clean, efficient	___ / 7
Pass DRC (no join nets)	___ / 5
Pass LVS (no join nets)	___ / 7
Schematics still pass test bench	___ / 5
Core routed to pad frame	___ / 3
GDS reads back and passes DRC & LVS	___ / 3
Report	**___ / 20**
Cover	___ / 1
Introduction	___ / 4
Specifications	___ / 2
Floorplan	___ / 4
Verification	___ / 2
Postfabrication test plan (if applicable)	___ / +2
Design Time	___ / 2
File Locations	___ / 2
References	___ / 1
Appendices	___ / 2