Harris

Hardware/Software Codesign for Wireless Systems (E168b) Syllabus

Spring 2007

Teaching Staff

Professor: David Money Harris Parsons 2374 x73623 David_Harris@hmc.edu

Schedule

Lecture: MW 1:15-2:30
Office Hours: TBD

I am in my office more often than not, so feel free to stop by even if I do not have official office hours.

Overview

This is an advanced class that builds on your previous digital design, programming, and systems experience. In this class, you will implement a GPS receiver on a high-end FPGA board. The FPGA contains two PowerPC microprocessors and oodles of configurable logic blocks and memory. You will use Matlab to model and validate the GPS receiver, then will use C on the PowerPC and Verilog on the FPGA to create the receiver. For a final project, you and a partner will propose and implement an enhancement to the receiver.

Texts

Required: E. Kaplan and C. Hegarty, *Understanding GPS: Principles and Applications*, 2nd ed, Artech House Publshers, 2005. This book covers GPS systems in substantial detail.

Optional: A. Kelley, I. Pohl, *A Book on C, 4th ed.*, Addison-Wesley, 1997. You will need to write reasonably sophisticated C programs. If you are unfamiliar with the language, this or similar books are recommended.

Optional: K. Borre et al., *A Software-Defined GPS and Galileo Receiver: A Single-Frequency Approach*, Birkhauser, 2007. This book contains a Matlab implementation of the GPS receiver that we will be building and has a succinct description of GPS systems. However, it is an honor code violation to refer to the Matlab code (e.g. on the enclosed DVD) when working on the class assignments because that would give an unfair advantage.

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e168b
Class email list: eng-168b-l

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-168b-l

Grading

Labs:	50%
Problem Sets:	20%
Final Project:	25%
In-class Activities:	5%

Tentative Schedule

The attached schedule is a tentative plan that may change during the semester. This is a new course, so changes are quite likely. The schedule lists reading from Kaplan associated with some lectures. You are expected to do the reading before class and be prepared to discuss it.

00000	17-Jan	Introduction and overview	1.1-1.10		
00001	22-Jan	C Programming: Pointers		Virtex Board Warmup	Lab 0 due
00010	24-Jan	Memory Mapped I/O		FPGA Bingo	PS 0 due
00011	29-Jan	Verilog: Test Benches		Hardware/Software Codesign	Lab 1 due
00100	31-Jan	Introduction to GPS systems	2.1-2.6	Geocache	PS 1 due
00101	5-Feb	GPS Signal Structure	4.1-4.4	Time-multiplexed correlator	Lab 2 due
00110	7-Feb	Acquisition	5.1-5.2	Gold codes	PS 2 due
	12-Feb	-- ISSCC, no Class ---			
00111	14-Feb	Tracking	5.3-5.5		
01000	19-Feb	PLLs, and DLLs		Acquisition	Lab 3 due
01001	21-Feb	Orbital Mechanics and Geodesy			
01010	26-Feb	Positioning	5.7	Tracking	Lab 4 due
01011	28-Feb	Real Time Systems			
01100	5-Mar	Validation, Test Plans		Positioning	Lab 5 due
01101	7-Mar	FPGAs: Timing analysis & floorplanning			
	12-Mar	-- Spring Break, no Class –			
	14-Mar	-- Spring Break, no Class –			
01110	19-Mar	VHDL		Hardware acquisition	Lab 6 due
01111	21-Mar	VHDL			
10000	26-Mar	VHDL		GPS receiver	Lab 7 due
10001	28-Mar	(Embedded Linux?)		VHDL	PS 3 due
10010	2-Apr				Project proposal
10011	4-Apr				
10100	9-Apr	Project presentations			
10101	11-Apr	Project presentations			Project status
10110	16-Apr				
10111	18-Apr				
11000	23-Apr	Project demonstrations			Project due
11001	25-Apr	Party			