



## FPGA Bingo

To familiarize yourself with the XUPV2P board, answer these questions:

- 1) What FPGA is on the Xilinx XUPV2P board?
- 2) How much does the board cost commercially? What is the academic price? Why do you think that they differ?
- 3) The CLBs on the FPGA are arranged in an array. How many rows and columns of CLBs are present? How many slices are in each CLB? How many 4-input lookup tables are in a slice? How many LUTs are available on the FPGA? How many flip-flops are in a slice? How many flip-flops are available on the FPGA?
- 4) Explain some of the other handy things in a slice.
- 5) How many PowerPC microprocessors are on the FPGA?
- 6) How many dedicated multipliers are on the FPGA? How big are they?
- 7) How many KB of Block RAM are available? How many ports are on each RAM block? What is the point of having more than one port? If the RAM is organized as an array of 32-bit words, how many words are available?
- 8) What is a DCM and why would you use one? How many are on the FPGA?
- 9) What power supply voltages are used by the FPGA on the board and what is the role of each one?
- 10) What are the main two unterminated 3.3V I/O standards supported by the FPGA? How do they differ?
- 11) How many user I/O pins are available?
- 12) What is the maximum operating frequency of a dedicated multiplier? Of a 32-bit adder? Of a single-ported block RAM? Of a linear feedback shift register with a critical path consisting of a 3-input XOR between two registers? Use the data for a speed grade -6 part; our chip is speed grade -7, which is slightly faster.