

# **Lecture 4: Nonideal Transistor Theory**

# Outline

- ❑ Nonideal Transistor Behavior
  - High Field Effects
    - Mobility Degradation
    - Velocity Saturation
  - Channel Length Modulation
  - Threshold Voltage Effects
    - Body Effect
    - Drain-Induced Barrier Lowering
    - Short Channel Effect
  - Leakage
    - Subthreshold Leakage
    - Gate Leakage
    - Junction Leakage
- ❑ Process and Environmental Variations

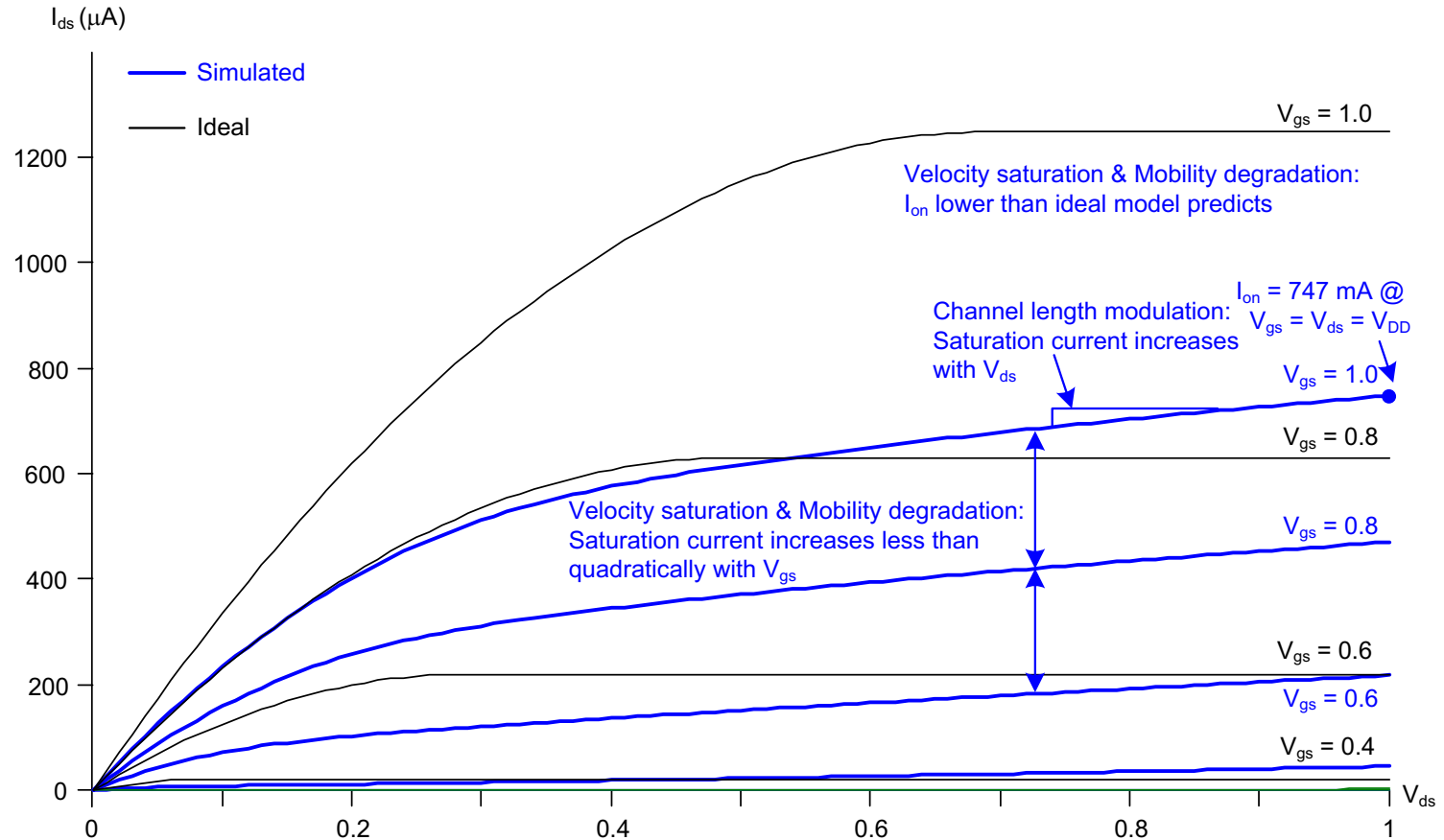
# Ideal Transistor I-V

- Shockley long-channel transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

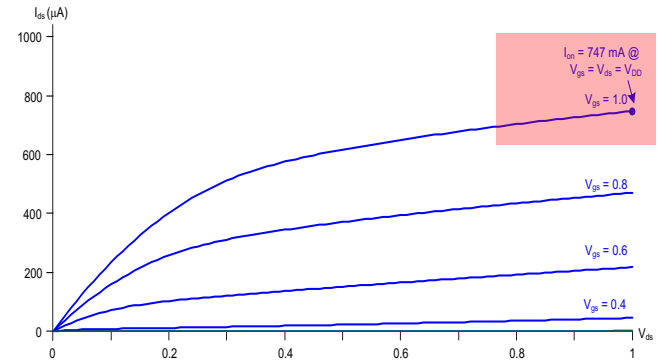
# Ideal vs. Simulated nMOS I-V Plot

□ 65 nm IBM process,  $V_{DD} = 1.0\text{ V}$

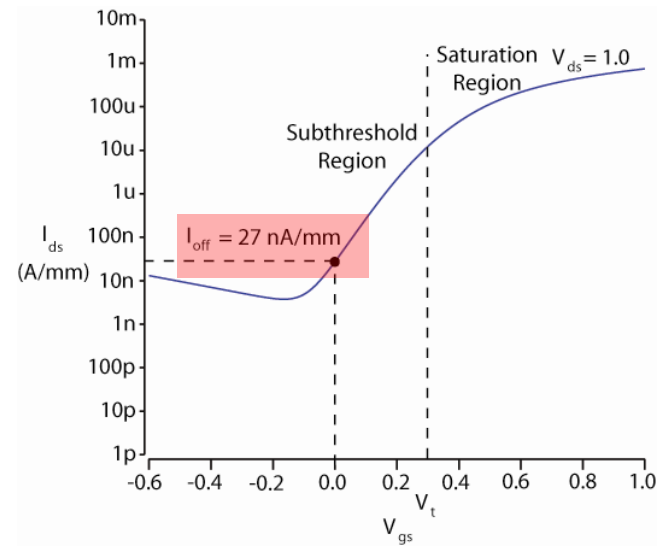


# ON and OFF Current

□  $I_{on} = I_{ds} @ V_{gs} = V_{ds} = V_{DD}$   
– Saturation



□  $I_{off} = I_{ds} @ V_{gs} = 0, V_{ds} = V_{DD}$   
– Cutoff



# Electric Fields Effects

- Vertical electric field:  $E_{\text{vert}} = \underline{\hspace{2cm}}$ 
  - Attracts carriers into channel
  - Long channel:  $Q_{\text{channel}}$  proportional to  $E_{\text{vert}}$
- Lateral electric field:  $E_{\text{lat}} = \underline{\hspace{2cm}}$ 
  - Accelerates carriers from drain to source
  - Long channel:  $v = \mu E_{\text{lat}}$

# Coffee Cart Analogy

- ❑ Tired student runs from VLSI lab to coffee cart
- ❑ Freshmen are pouring out of the physics lecture hall
- ❑  $V_{ds}$  is how long you have been up
  - Your velocity = fatigue  $\times$  mobility
- ❑  $V_{gs}$  is a wind blowing you against the glass ( $\text{SiO}_2$ ) wall
- ❑ At high  $V_{gs}$ , you are buffeted against the wall
  - *Mobility degradation*
- ❑ At high  $V_{ds}$ , you scatter off freshmen, fall down, get up
  - *Velocity saturation*
    - Don't confuse this with the saturation region

# Mobility Degradation

- High  $E_{\text{vert}}$  effectively reduces mobility
  - Collisions with oxide interface

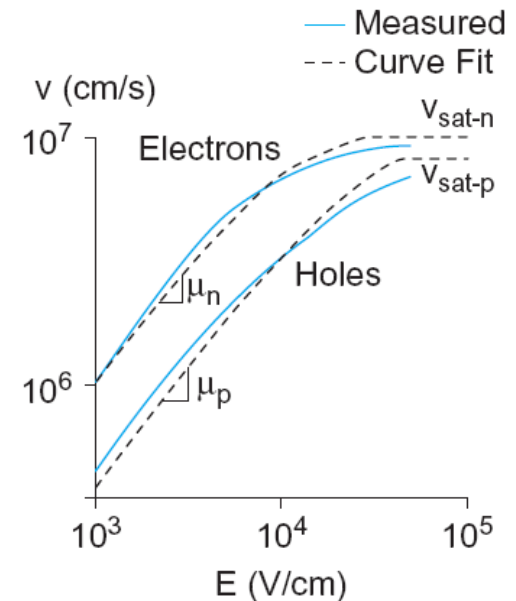
$$\mu_{\text{eff}-n} = \frac{540 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}}{1 + \left( \frac{V_{gs} + V_t}{0.54 \frac{\text{V}}{\text{nm}} t_{\text{ox}}} \right)^{1.85}} \quad \mu_{\text{eff}-p} = \frac{185 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}}{1 + \frac{|V_{gs} + 1.5V_t|}{0.338 \frac{\text{V}}{\text{nm}} t_{\text{ox}}}}$$



# Velocity Saturation

- At high  $E_{\text{lat}}$ , carrier velocity rolls off
  - Carriers scatter off atoms in silicon lattice
  - Velocity reaches  $v_{\text{sat}}$ 
    - Electrons:  $10^7$  cm/s
    - Holes:  $8 \times 10^6$  cm/s
  - Better model

$$v = \begin{cases} \frac{\mu_{\text{eff}} E}{1 + \frac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases} \quad E_c = \frac{2v_{\text{sat}}}{\mu_{\text{eff}}}$$



# Vel Sat I-V Effects

- ❑ Ideal transistor ON current increases with  $V_{DD}^2$

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2} = \frac{\beta}{2} (V_{gs} - V_t)^2$$

- ❑ Velocity-saturated ON current increases with  $V_{DD}$

$$I_{ds} = C_{ox} W (V_{gs} - V_t) v_{sat}$$

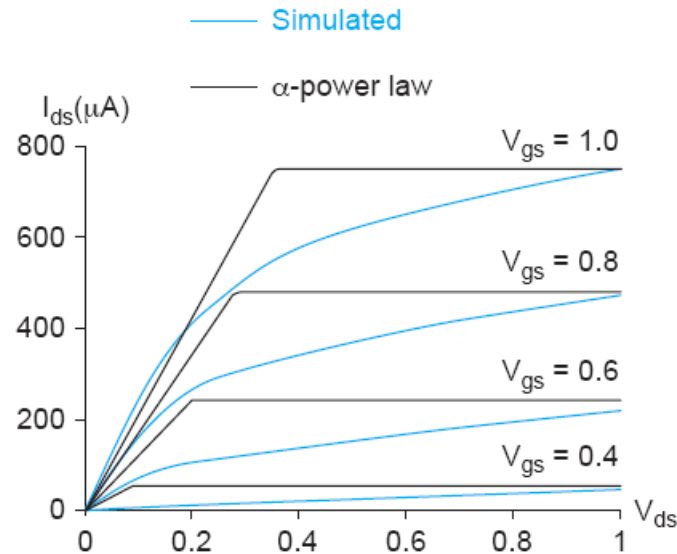
- ❑ Real transistors are partially velocity saturated
  - Approximate with  $\alpha$ -power law model
  - $I_{ds}$  scales with  $V_{DD}^\alpha$
  - $1 < \alpha < 2$  determined empirically ( $\approx 1.3$  for 65 nm)

# $\alpha$ -Power Model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ I_{dsat} \frac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} & \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

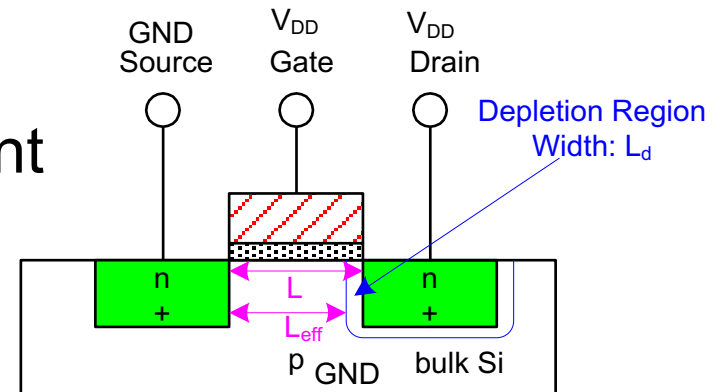
$$I_{dsat} = P_c \frac{\beta}{2} (V_{gs} - V_t)^\alpha$$

$$V_{dsat} = P_v (V_{gs} - V_t)^{\alpha/2}$$



# Channel Length Modulation

- ❑ Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion  $L_d$  region grows with reverse bias
  - $L_{\text{eff}} = L - L_d$
- ❑ Shorter  $L_{\text{eff}}$  gives \_\_\_\_\_ current
  - $I_{\text{ds}}$  \_\_\_\_\_ with  $V_{\text{ds}}$
  - Even in saturation



# Chan Length Mod I-V

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2 (1 + \lambda V_{ds})$$

- $\lambda =$  *channel length modulation coefficient*
  - not feature size
  - Empirically fit to I-V characteristics

# Threshold Voltage Effects

- ❑  $V_t$  is  $V_{gs}$  for which the channel starts to invert
- ❑ Ideal models assumed  $V_t$  is constant
- ❑ Really depends (weakly) on almost everything else:
  - Body voltage: *Body Effect*
  - Drain voltage: *Drain-Induced Barrier Lowering*
  - Channel length: *Short Channel Effect*

# Body Effect

- ❑ Body is a fourth transistor terminal
- ❑  $V_{sb}$  affects the charge required to invert the channel
  - Increasing  $V_s$  or decreasing  $V_b$  increases  $V_t$

$$V_t = V_{t0} + \gamma \left( \sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

- ❑  $V_{t0}$  = nominal threshold voltage
- ❑  $\phi_s$  = *surface potential* at threshold

$$\phi_s = 2v_T \ln \frac{N_A}{n_i}$$

- Depends on doping level  $N_A$
  - And intrinsic carrier concentration  $n_i$
- ❑  $\gamma$  = *body effect coefficient*

$$\gamma = \frac{t_{ox}}{\epsilon_{ox}} \sqrt{2q\epsilon_{si}N_A} = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}}$$

# Body Effect Cont.

- For small source-to-body voltage, treat as linear

$$V_t = V_{t0} + k_\gamma V_{sb}$$

$$k_\gamma = \frac{\gamma}{2\sqrt{\phi_s}} = \frac{\sqrt{\frac{q\epsilon_{si}N_A}{v_T \ln \frac{N_A}{n_i}}}}{2C_{ox}}$$

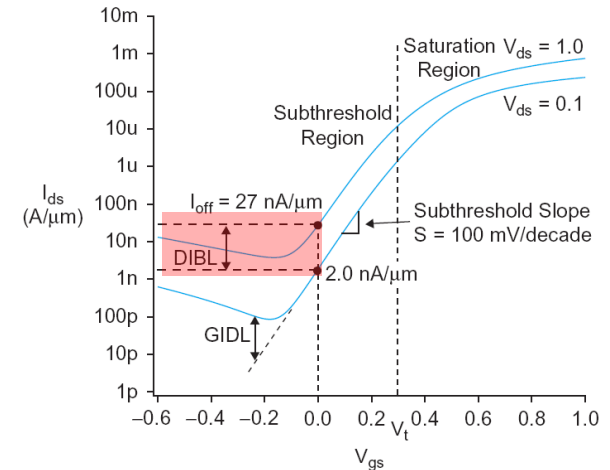


# DIBL

- ❑ Electric field from drain affects channel
- ❑ More pronounced in small transistors where the drain is closer to the channel
- ❑ Drain-Induced Barrier Lowering
  - Drain voltage also affect  $V_t$

$$V_t' = V_t - \eta V_{ds}$$

- ❑ High drain voltage causes current to \_\_\_\_\_



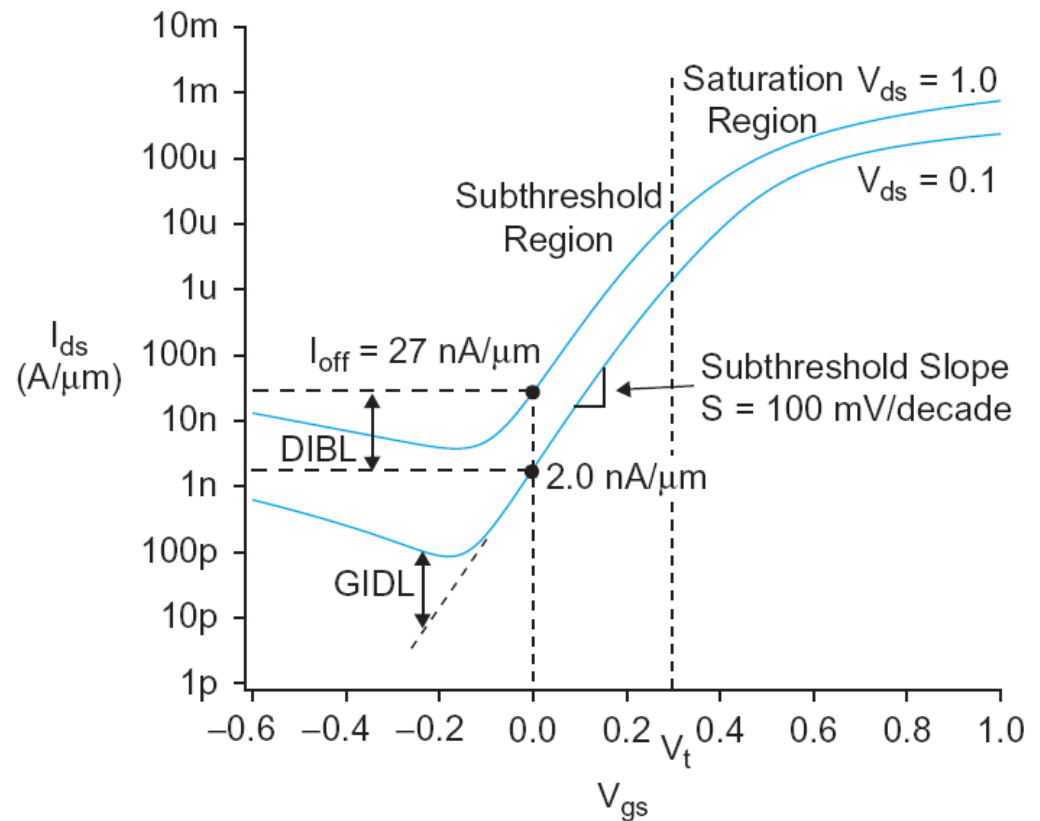
# Short Channel Effect

- ❑ In small transistors, source/drain depletion regions extend into the channel
  - Impacts the amount of charge required to invert the channel
  - And thus makes  $V_t$  a function of channel length
- ❑ Short channel effect:  $V_t$  increases with  $L$ 
  - Some processes exhibit a reverse short channel effect in which  $V_t$  decreases with  $L$

# Leakage

- ❑ What about current in cutoff?
- ❑ Simulated results
- ❑ What differs?

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# Leakage Sources

- ❑ Subthreshold conduction
  - Transistors can't abruptly turn ON or OFF
  - Dominant source in contemporary transistors
- ❑ Gate leakage
  - Tunneling through ultrathin gate dielectric
- ❑ Junction leakage
  - Reverse-biased PN junction diode current

# Subthreshold Leakage

- Subthreshold leakage exponential with  $V_{gs}$

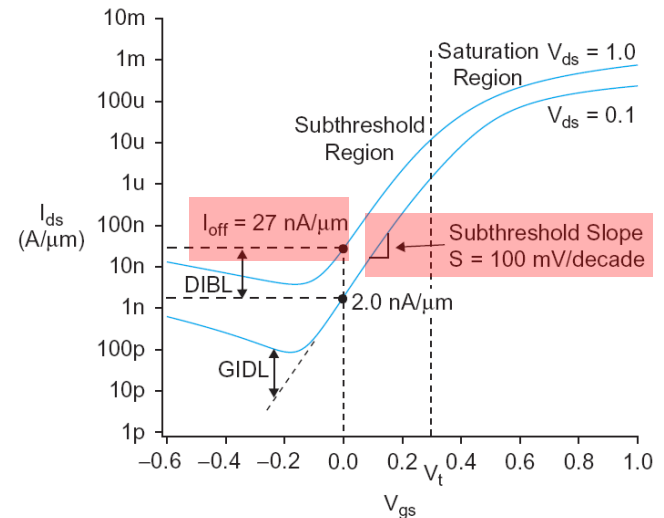
$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{t0} + \eta V_{ds} - k_{\gamma} V_{sb}}{n v_T}} \left( 1 - e^{-\frac{V_{ds}}{v_T}} \right)$$

- $n$  is process dependent
  - typically 1.3-1.7
- Rewrite relative to  $I_{off}$  on log scale

$$I_{ds} = I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{dd}) - k_{\gamma} V_{sb}}{S}} \left( 1 - e^{-\frac{V_{ds}}{v_t}} \right)$$

$$S = \left[ \frac{d(\log_{10} I_{ds})}{dV_{gs}} \right]^{-1} = n v_T \ln 10$$

- $S \approx 100$  mV/decade @ room temperature



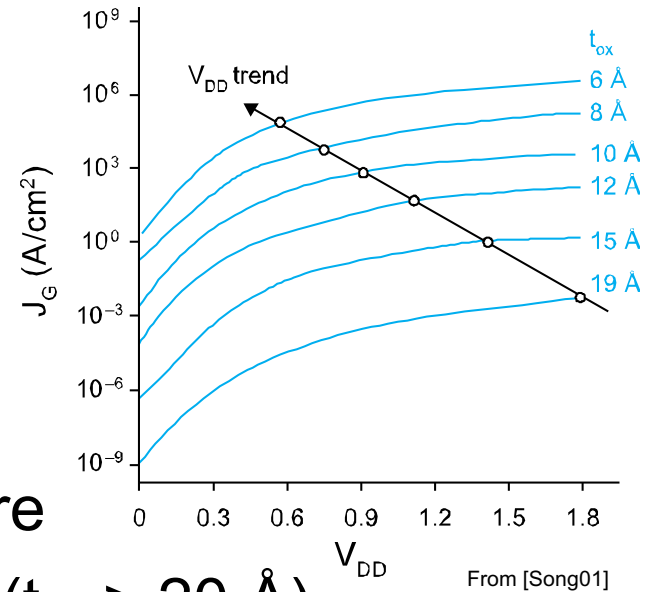
# Gate Leakage

- ❑ Carriers tunnel through very thin gate oxides
- ❑ Exponentially sensitive to  $t_{ox}$  and  $V_{DD}$

$$I_{gate} = WA \left( \frac{V_{DD}}{t_{ox}} \right)^2 e^{-B \frac{t_{ox}}{V_{DD}}}$$

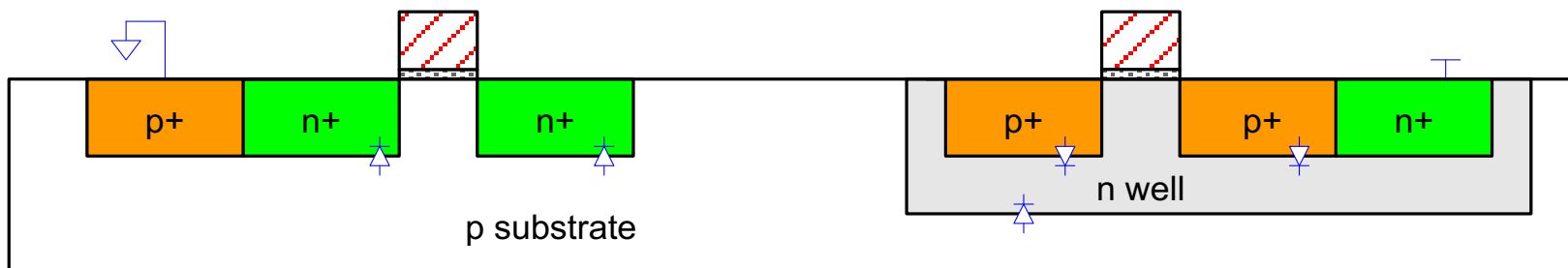
- A and B are tech constants
- Greater for electrons
  - So nMOS gates leak more

- ❑ Negligible for older processes ( $t_{ox} > 20 \text{ \AA}$ )
- ❑ Critically important at 65 nm and below ( $t_{ox} \approx 10.5 \text{ \AA}$ )



# Junction Leakage

- ❑ Reverse-biased p-n junctions have some leakage
  - Ordinary diode leakage
  - Band-to-band tunneling (BTBT)
  - Gate-induced drain leakage (GIDL)



# Diode Leakage

- ❑ Reverse-biased p-n junctions have some leakage

$$I_D = I_S \left( e^{\frac{V_D}{V_T}} - 1 \right)$$

- ❑ At any significant negative diode voltage,  $I_D = -I_S$
- ❑  $I_S$  depends on doping levels
  - And area and perimeter of diffusion regions
  - Typically  $< 1 \text{ fA}/\mu\text{m}^2$  (negligible)



# Band-to-Band Tunneling

- ❑ Tunneling across heavily doped p-n junctions
  - Especially sidewall between drain & channel when *halo doping* is used to increase  $V_t$
- ❑ Increases junction leakage to significant levels

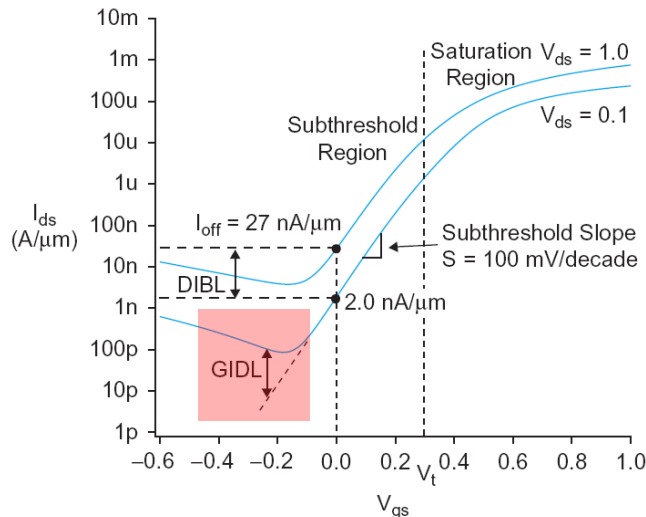
$$I_{BTBT} = WX_j A \frac{E_j}{E_g^{0.5}} V_{dd} e^{-B \frac{E_g^{1.5}}{E_j}}$$

$$E_j = \sqrt{\frac{2qN_{halo}N_{sd}}{\epsilon(N_{halo} + N_{sd})}} \left( V_{DD} + v_T \ln \frac{N_{halo}N_{sd}}{n_i^2} \right)$$

- $X_j$ : sidewall junction depth
- $E_g$ : bandgap voltage
- A, B: tech constants

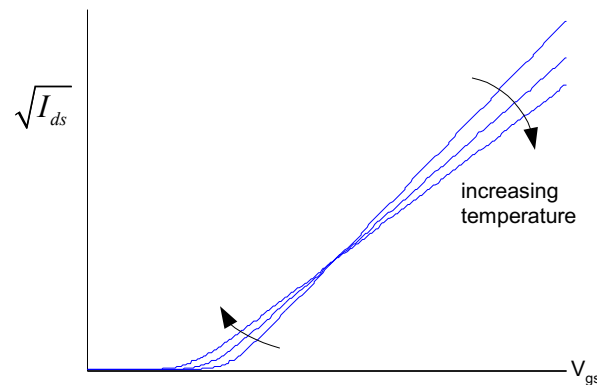
# Gate-Induced Drain Leakage

- ❑ Occurs at overlap between gate and drain
  - Most pronounced when drain is at  $V_{DD}$ , gate is at a negative voltage
  - Thwarts efforts to reduce subthreshold leakage using a negative gate voltage



# Temperature Sensitivity

- ❑ Increasing temperature
  - Reduces mobility
  - Reduces  $V_t$
- ❑  $I_{ON}$  \_\_\_\_\_ with temperature
- ❑  $I_{OFF}$  \_\_\_\_\_ with temperature

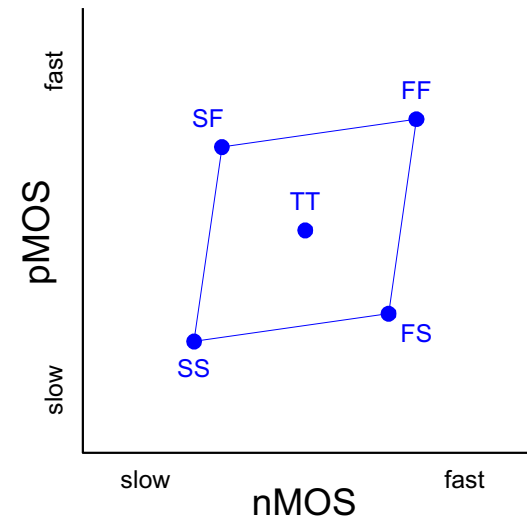


# So What?

- ❑ So what if transistors are not ideal?
  - They still behave like switches.
- ❑ But these effects matter for...
  - Supply voltage choice
  - Logical effort
  - Quiescent power consumption
  - Pass transistors
  - Temperature of operation

# Parameter Variation

- ❑ Transistors have uncertainty in parameters
  - Process:  $L_{\text{eff}}$ ,  $V_t$ ,  $t_{\text{ox}}$  of nMOS and pMOS
  - Vary around typical (T) values
- ❑ Fast (F)
  - $L_{\text{eff}}$ : \_\_\_\_\_
  - $V_t$ : \_\_\_\_\_
  - $t_{\text{ox}}$ : \_\_\_\_\_
- ❑ Slow (S): opposite
- ❑ Not all parameters are independent for nMOS and pMOS



# Environmental Variation

- ❑  $V_{DD}$  and  $T$  also vary in time and space
- ❑ Fast:
  - $V_{DD}$ : \_\_\_\_\_
  - $T$ : \_\_\_\_\_

Corner	Voltage	Temperature
F		
T	1.8	70 C
S		

# Process Corners

- ❑ Process corners describe worst case variations
  - If a design works in all corners, it will probably work for any variation.
- ❑ Describe corner with four letters (T, F, S)
  - nMOS speed
  - pMOS speed
  - Voltage
  - Temperature

# Important Corners

- ❑ Some critical simulation corners include

Purpose	nMOS	pMOS	$V_{DD}$	Temp
Cycle time				
Power				
Subthreshold leakage				