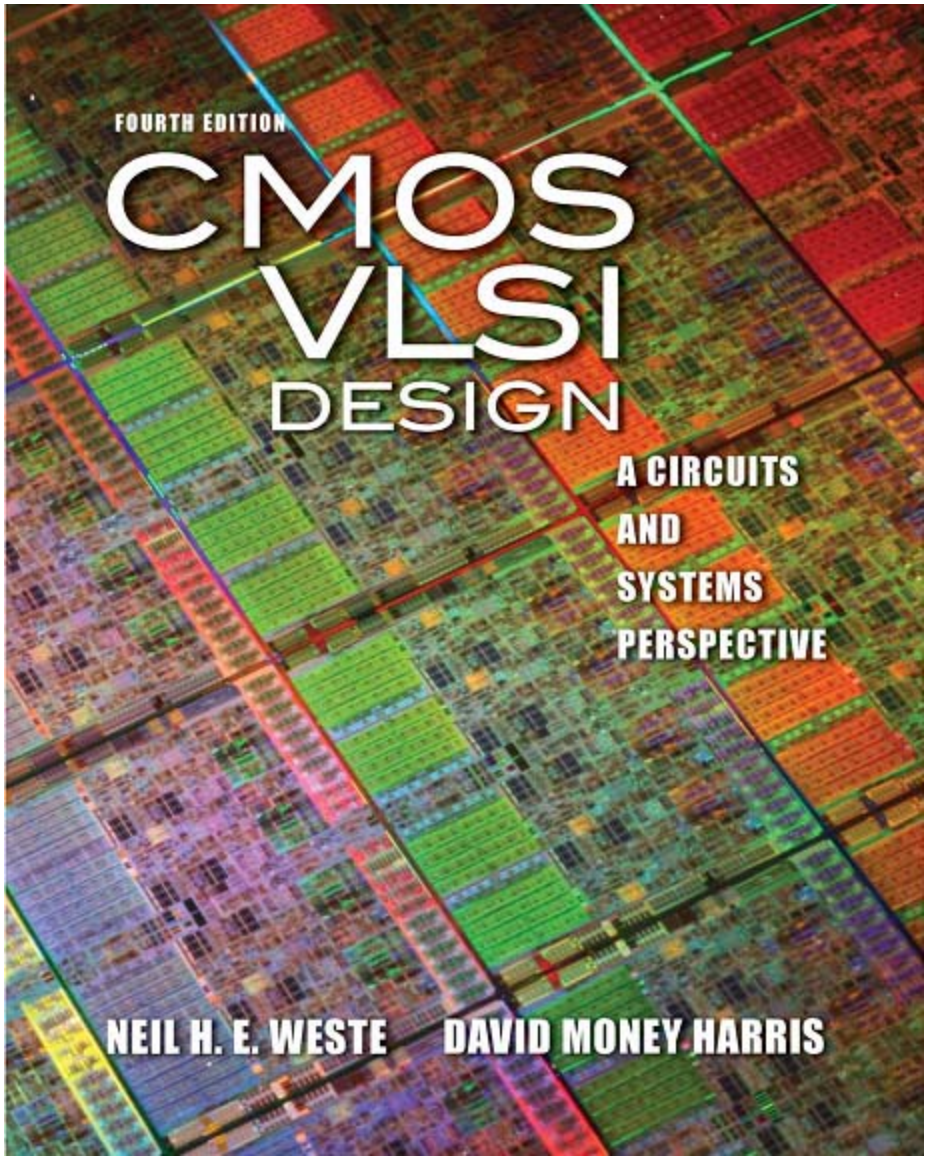


Lecture 20: PLLs and DLLs

Outline

- Clock System Architecture
- Phase-Locked Loops
- Delay-Locked Loops

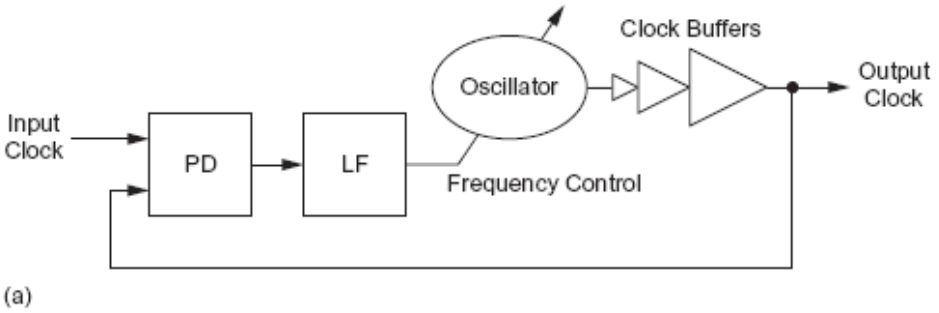
Clock Generation

- Low frequency:
  - Buffer input clock and drive to all registers
- High frequency
  - Buffer delay introduces large skew relative to input clocks
    - Makes it difficult to sample input data
  - Distributing a very fast clock on a PCB is hard

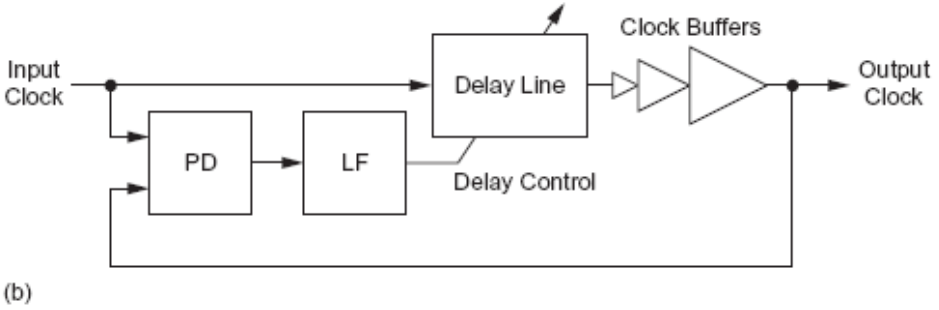
Zero-Delay Buffer

- If the periodic clock is delayed by T_c, it is indistinguishable from the original clock
- Build feedback system to guarantee this delay

Phase-Locked Loop (PLL)

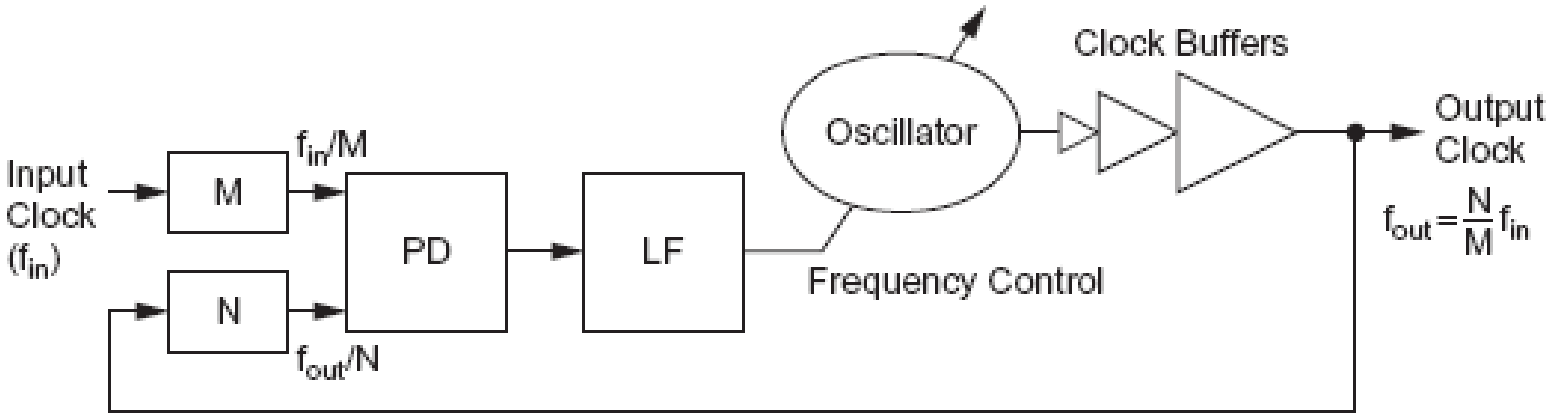


Delay-Locked Loop (PLL)



Frequency Multiplication

- PLLs can multiply the clock frequency

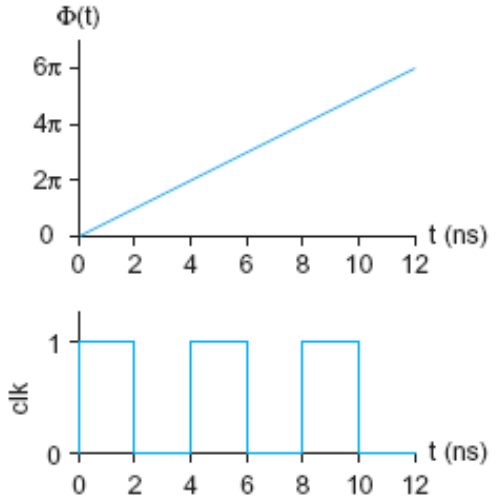


Phase and Frequency

- Analyze PLLs and DLLs in term of phase Φ(t) rather than voltage v(t)

$$\text{clk} = \begin{cases} 1 & \Phi(t) \bmod 2\pi < \pi \\ 0 & \Phi(t) \bmod 2\pi \geq \pi \end{cases}$$

$$\Phi(t) = 2\pi \int_0^t f(t) dt$$



- Input and output clocks may deviate from locked phase
  - Small signal analysis

$$\Phi_{\text{in}}(t) = \Phi(t) + \Delta\Phi_{\text{in}}(t)$$

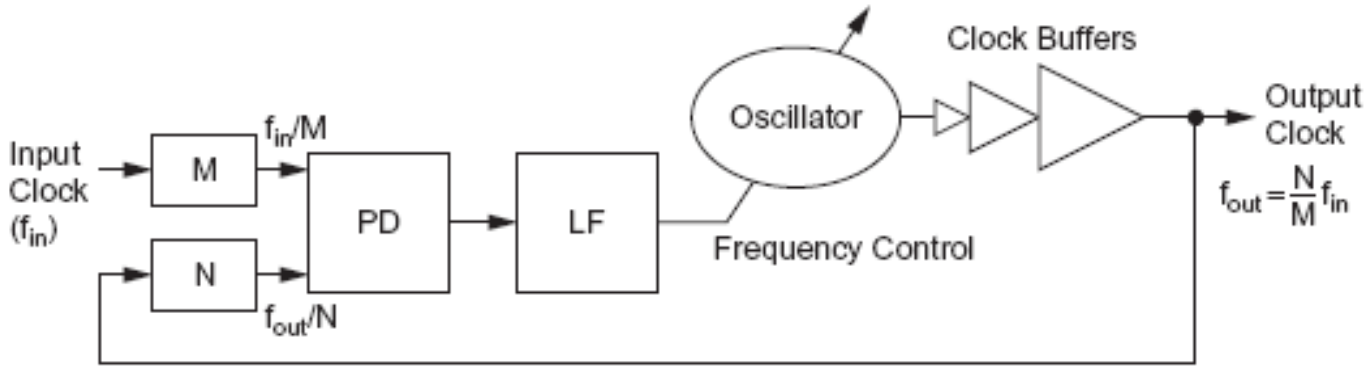
$$\Phi_{\text{out}}(t) = N\Phi(t) + \Delta\Phi_{\text{out}}(t)$$

Linear System Model

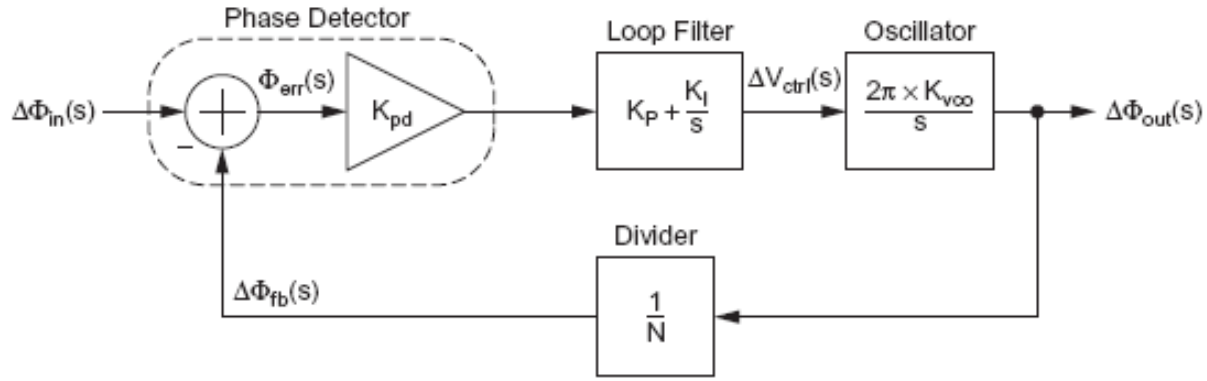
- Treat PLL/DLL as a linear system
  - Compute deviation DF from locked position
  - Assume small deviations from locked
  - Treat system as linear for these small changes
- Analysis is not valid far from lock
  - e.g. during acquisition at startup
- Continuous time assumption
  - PLL/DLL is really a discrete time system
    - Updates once per cycle
  - If the bandwidth << 1/10 clock freq, treat as continuous
- Use Laplace transforms and standard analysis of linear continuous-time feedback control systems

Phase-Locked Loop (PLL)

- System

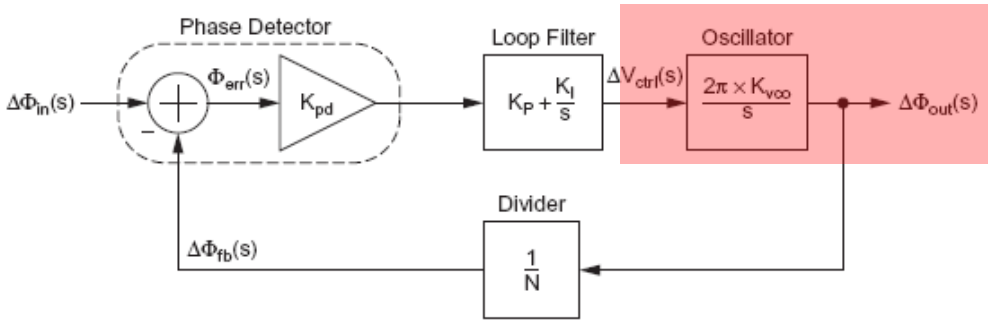


- Linear Model



Voltage-Controlled Oscillator

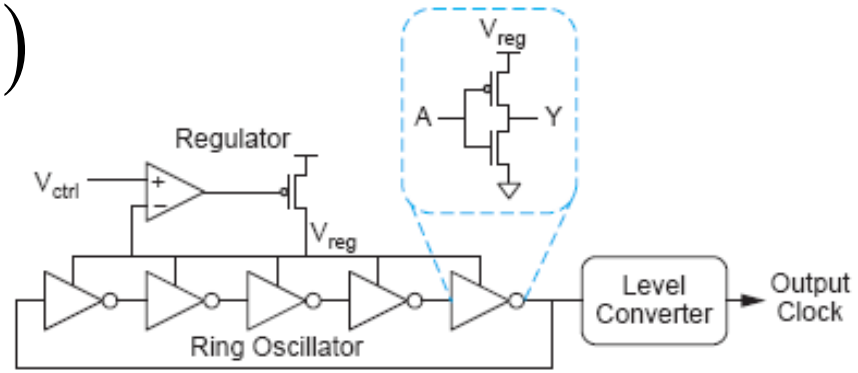
- VCO

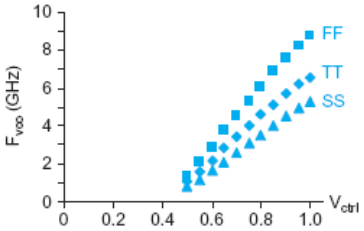


$$V_{\text{ctrl}}(t) = V_{\text{ctrl0}} + \Delta V_{\text{ctrl}}(t)$$

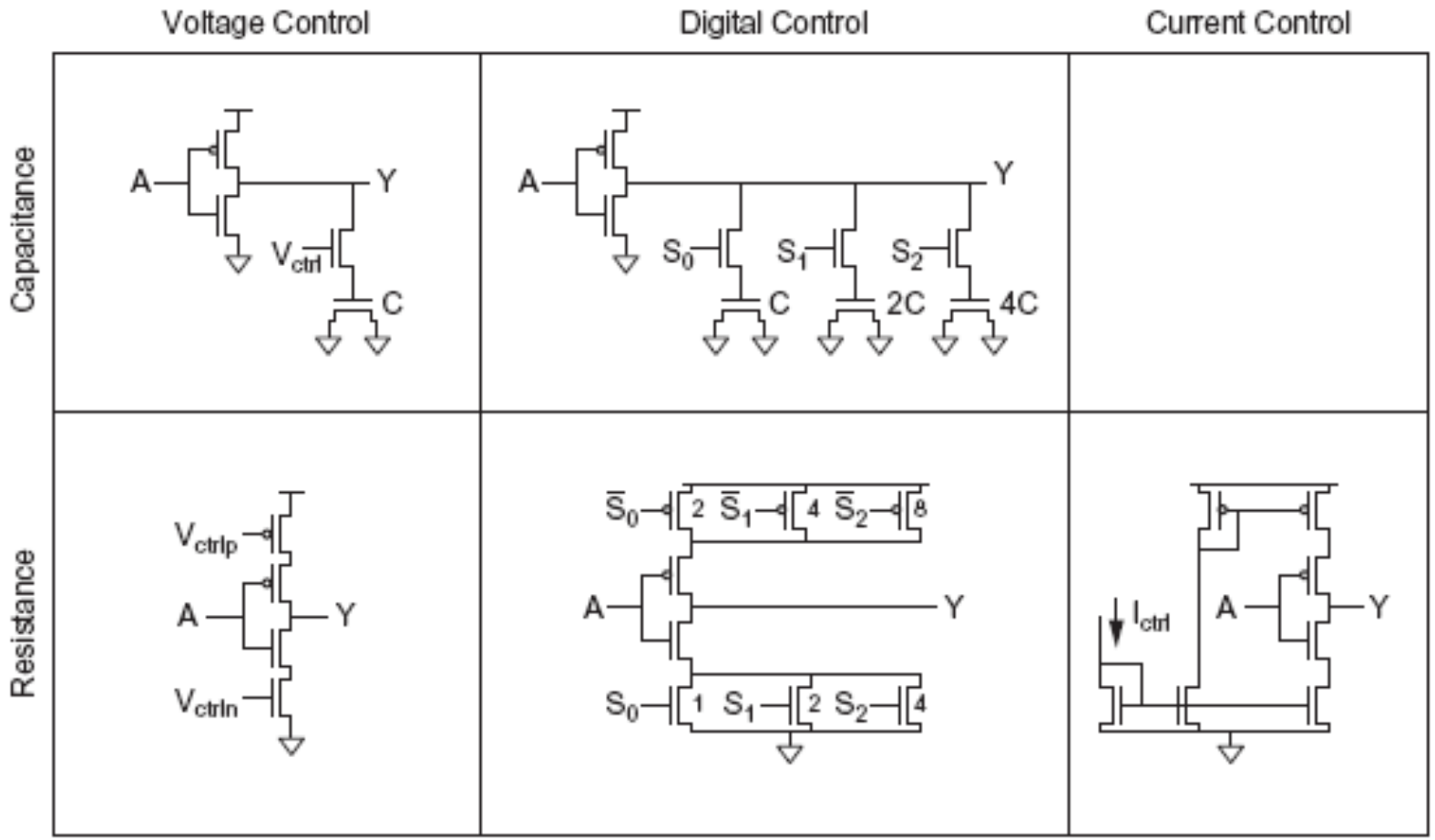
$$\frac{\Delta f_{out}}{\Delta V_{\text{ctrl}}} = K_{vco}$$

$$\frac{\Delta\Phi_{out}(s)}{\Delta V_{ctrl}(s)} = \frac{2\pi K_{vco}}{s}$$



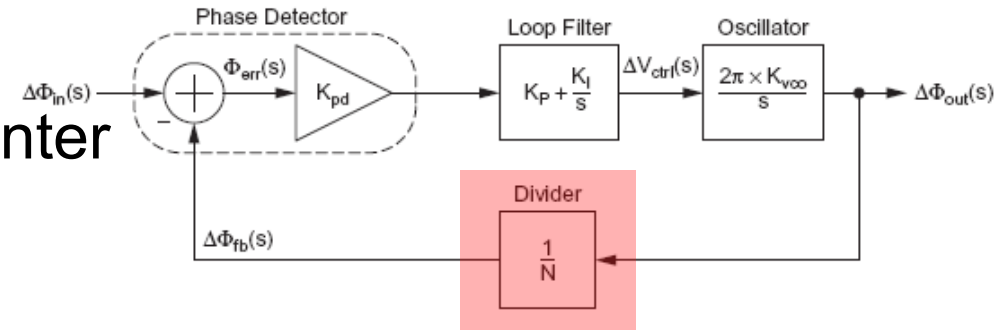


Alternative Delay Elements



Frequency Divider

- Divide clock by N
  - Use mod-N counter

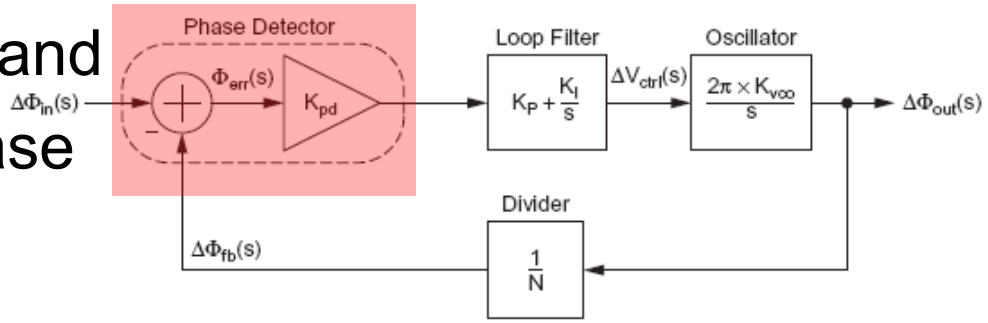


$$\Delta f_{fb} = \frac{\Delta f_{out}}{N}$$

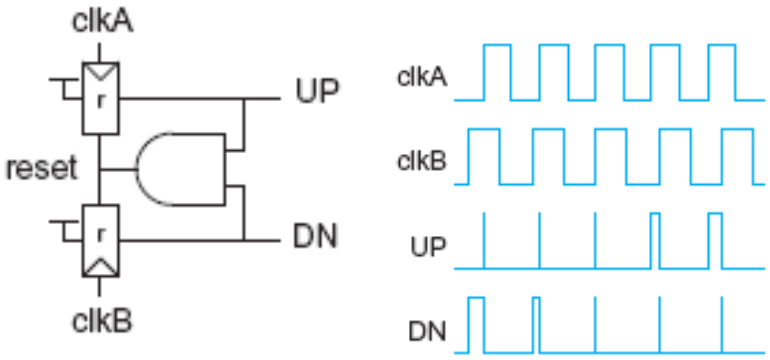
$$\Delta \Phi_{fb} = \frac{\Delta \Phi_{out}}{N}$$

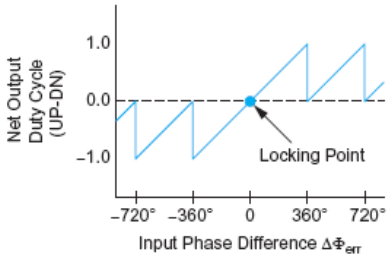
Phase Detector

- Difference of input and feedback clock phase



- Often built from phase-frequency detector (PFD)

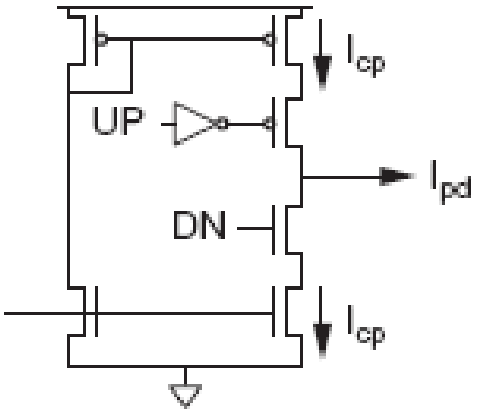




Phase Detector

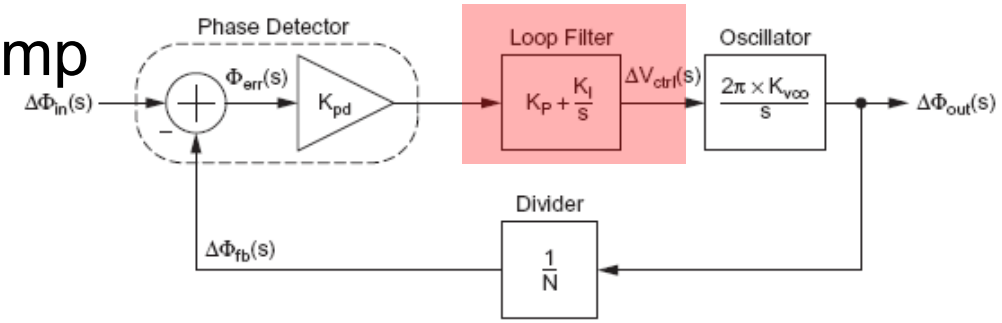
- Convert up and down pulses into current proportional to phase error using a charge pump

$$\frac{I_{pd}(s)}{\Phi_{\text{err}}(s)} = \frac{I_{\text{cp}}}{2\pi} = K_{pd}$$



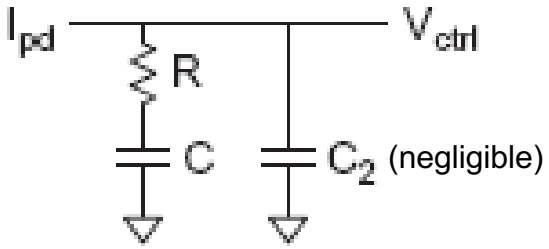
Loop Filter

- Convert charge pump current into V_{ctrl}



- Use proportional-integral control (PI) to generate a control signal dependent on the error and its integral
  - Drives error to 0

$$\frac{V_{\text{ctrl}}(s)}{I_{\text{pd}}(s)} = \frac{1}{sC} + R$$



PLL Loop Dynamics

- Closed loop transfer function of PLL

$$H(s) = \frac{\Delta\Phi_{\text{out}}(s)}{\Delta\Phi_{\text{in}}(s)} = \frac{K_{pd}\left(R + \frac{1}{sC}\right)\frac{2\pi K_{\text{vco}}}{s}}{1 + \frac{1}{N}K_{pd}\left(R + \frac{1}{sC}\right)\frac{2\pi K_{\text{vco}}}{s}}$$

- This is a second order system

$$H(s) = N\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \omega_n = \sqrt{\frac{I_{cp}K_{\text{vco}}}{NC}}$$

$$\zeta = \frac{\omega_n}{2}RC$$

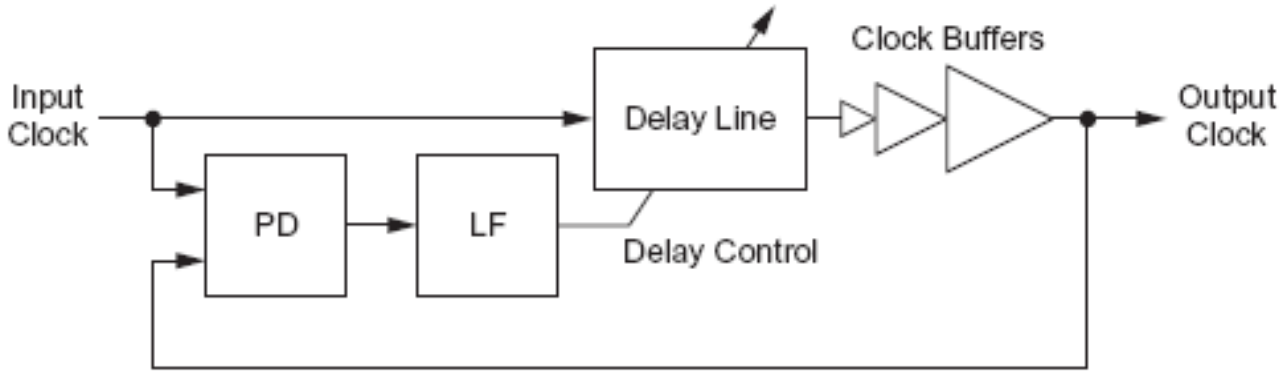
- ω_n indicates loop bandwidth
- ζ indicates damping; choose 0.7 – 1 to avoid ringing

Delay Locked Loop

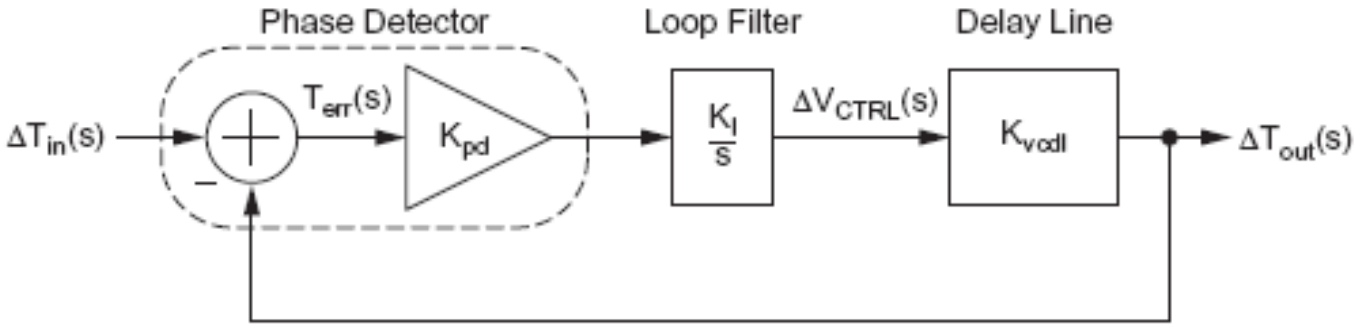
- Delays input clock rather than creating a new clock with an oscillator
- Cannot perform frequency multiplication
- More stable and easier to design
  - 1st order rather than 2nd
- State variable is now time (T)
  - Locks when loop delay is exactly T_c
  - Deviations of ΔT from locked value

Delay-Locked Loop (DLL)

- System

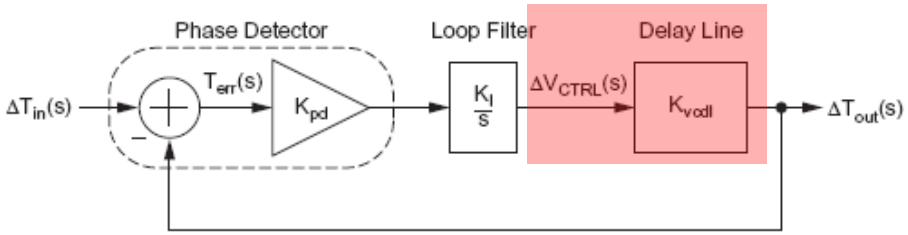


- Linear Model



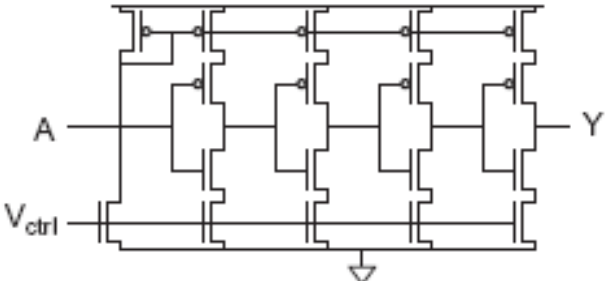
Delay Line

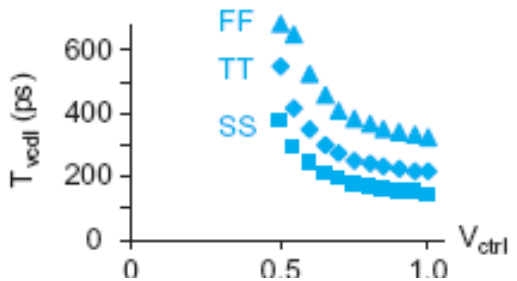
- Delay input clock



- Typically use voltage-controlled delay line

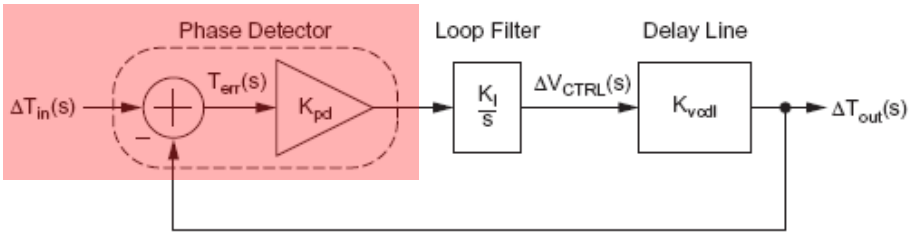
$$\frac{\Delta T_{\text{out}}(s)}{\Delta V_{\text{ctrl}}(s)} = K_{vcdl}$$





Phase Detector

- Detect phase error

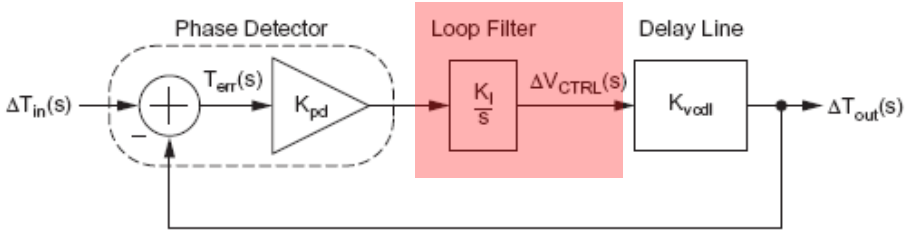


- Typically use PFD and charge pump, as in PLL

$$\frac{I_{pd}(s)}{T_{\text{err}}(s)} = \frac{I_{cp}}{T_c}$$

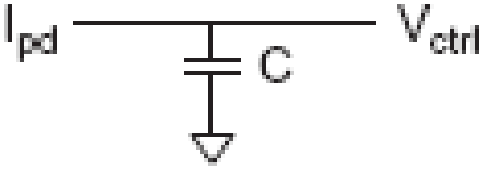
Loop Filter

- Convert error current into control voltage



- Integral control is sufficient
- Typically use a capacitor as the loop filter

$$\frac{\Delta V_{\text{ctrl}}(s)}{I_{pd}(s)} = \frac{K_I}{s} = \frac{1}{sC}$$



DLL Loop Dynamics

- Closed loop transfer function of DLL

$$H(s) = \frac{\Delta T_{\text{out}}(s)}{\Delta T_{\text{in}}(s)} = \frac{1}{s\tau + 1}$$

- This is a first order system

$$\tau = \frac{1}{K_{pd} K_I K_{vcdl}} = \frac{C T_c}{I_{cp} K_{vcdl}}$$

- τ indicates time constant (inverse of bandwidth)
  - Choose at least $10T_c$ for continuous time approx.