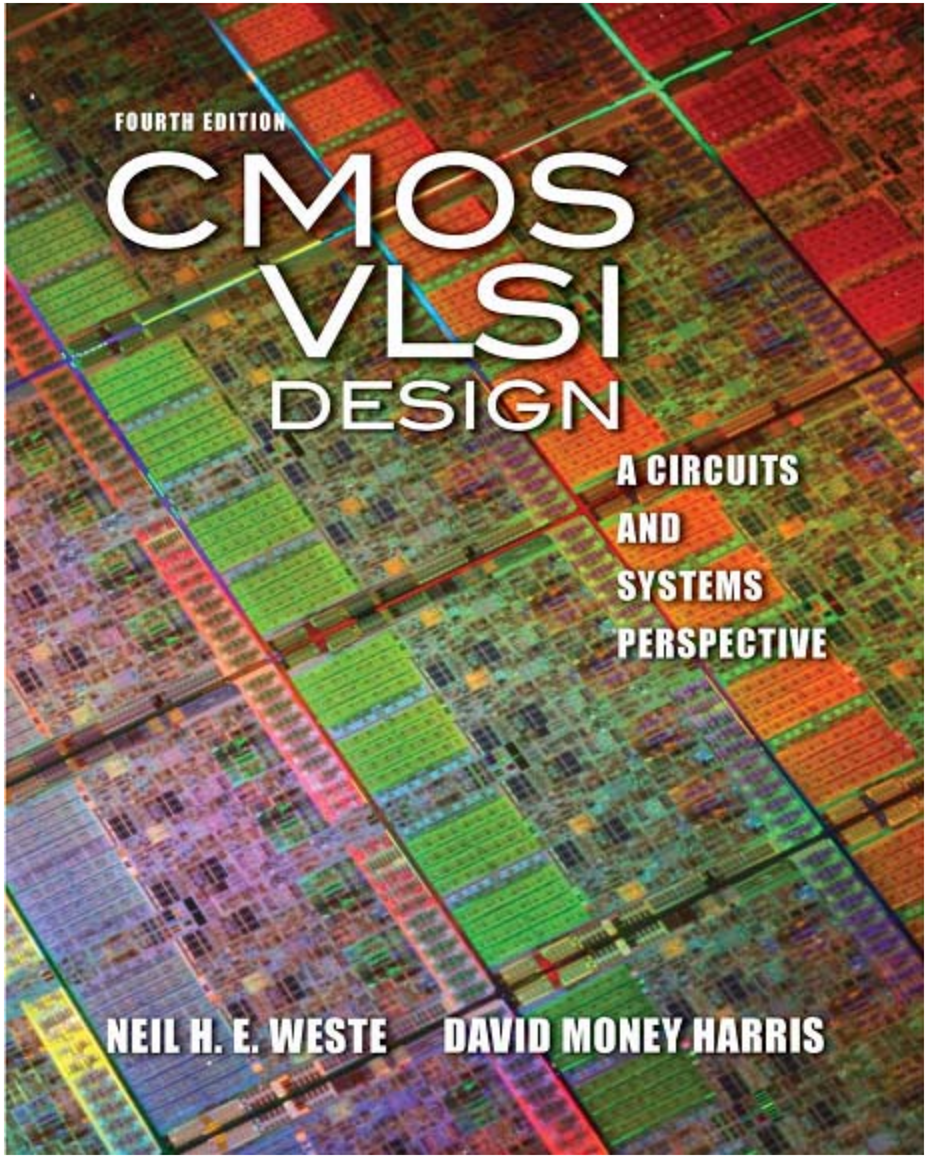


Lecture 18: Circuit Pitfalls

Outline

- Variation
- Noise Budgets
- Reliability
- Circuit Pitfalls

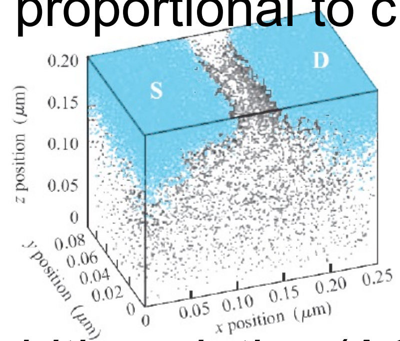
Variation

- Process
  - Threshold
  - Channel length
  - Interconnect dimensions
- Environment
  - Voltage
  - Temperature
- Aging / Wearout

Process Variation

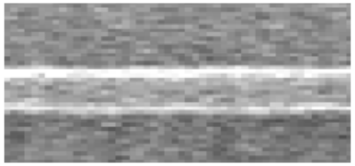
- Threshold Voltage
  - Depends on placement of dopants in channel
  - Standard deviation inversely proportional to channel area

$$\sigma_{V_t} = \frac{t_{ox}}{\varepsilon_{ox}} \frac{\sqrt[4]{q^3 \varepsilon_{si} \phi_b N_a}}{\sqrt{2LW}} = \frac{A_{V_t}}{\sqrt{LW}}$$

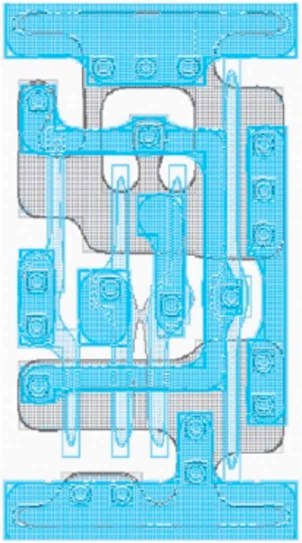


[Bernstein06]

- Channel Length
  - Systematic *across-chip linewidth variation* (ACLV)
  - Random line edge roughness (LER)



Courtesy Texas Instruments

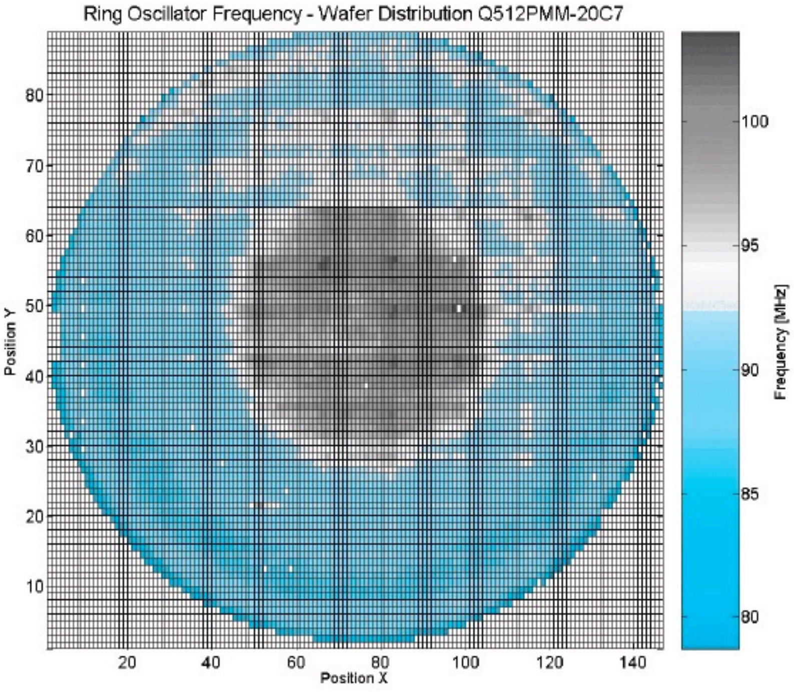


Courtesy Larry Pileggi

- Interconnect
  - Etching variations affect w, s, h

Spatial Distribution

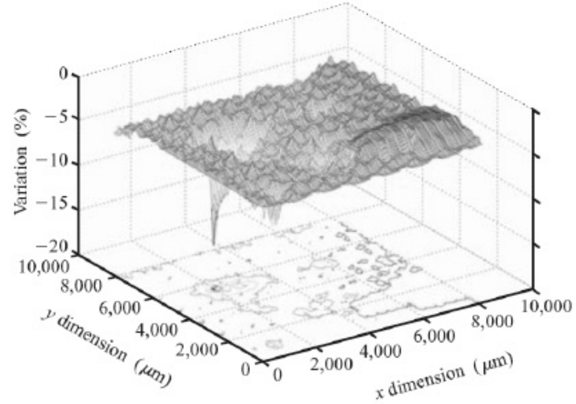
- Variations show spatial correlation
  - *Lot-to-lot* (L2L)
  - *Wafer-to-wafer* (W2W)
  - *Die-to-die* (D2D) / *inter-die*
  - *Within-die* (WID) / *intradie*
- Closer transistors match better



Courtesy M. Pelgrom

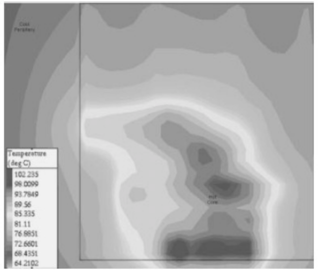
Environmental Variation

- Voltage
  - V_{DD} is usually designed +/- 10%
  - Regulator error
  - On-chip droop from switching activity
- Temperature
  - Ambient temperature ranges
  - On-die temperature elevated by chip power consumption



Courtesy IBM

Standard	Minimum	Maximum
Commercial	0 °C	70 °C
Industrial	−40 °C	85 °C
Military	−55 °C	125 °C



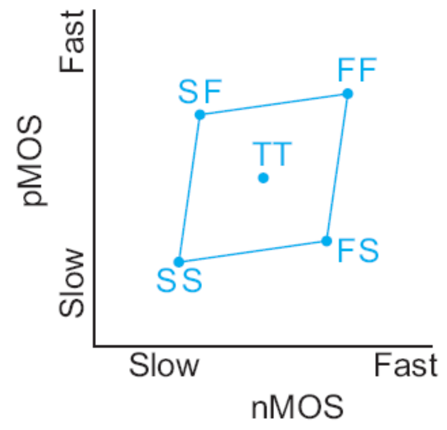
[Harris01b]

Aging

- Transistors change over time as they wear out
  - Hot carriers
  - Negative bias temperature instability
  - Time-dependent dielectric breakdown
- Causes threshold voltage changes
- More on this later…

Process Corners

- Model extremes of process variations in simulation
- Corners
  - Typical (T)
  - Fast (F)
  - Slow (S)
- Factors
  - nMOS speed
  - pMOS speed
  - Wire
  - Voltage
  - Temperature



Corner	Voltage	Temperature
F	1.98	0 °C
T	1.8	70 °C
S	1.62	125 °C

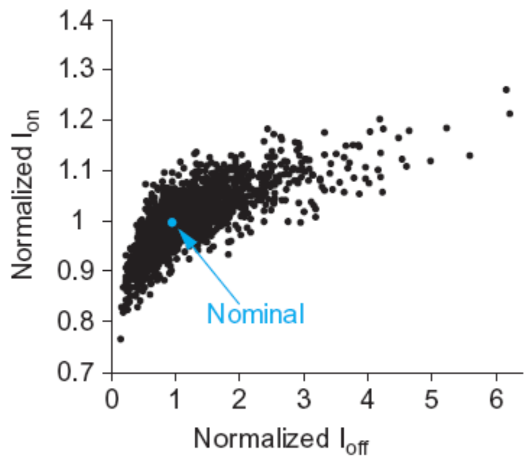
Corner Checks

- Circuits are simulated in different corners to verify different performance and correctness specifications

Corner					Purpose
nMOS	pMOS	Wire	V_{DD}	Temp	
T	T	T	S	S	Timing specifications (binned parts)
S	S	S	S	S	Timing specifications (conservative)
F	F	F	F	F	Race conditions, hold time constraints, pulse collapse, noise
S	S	?	F	S	Dynamic power
F	F	F	F	S	Subthreshold leakage noise and power, overall noise analysis
S	S	F	S	S	Races of gates against wires
F	F	S	F	F	Races of wires against gates
S	F	T	F	F	Pseudo-nMOS and ratioed circuits noise margins, memory read/write, race of pMOS against nMOS
F	S	T	F	F	Ratioed circuits, memory read/write, race of nMOS against pMOS

Monte Carlo Simulation

- As process variation increases, the worst-case corners become too pessimistic for practical design
- Monte Carlo: repeated simulations with parameters randomly varied each time
- Look at scatter plot of results to predict yield
- Ex: impact of V_t variation
  - ON-current
  - leakage

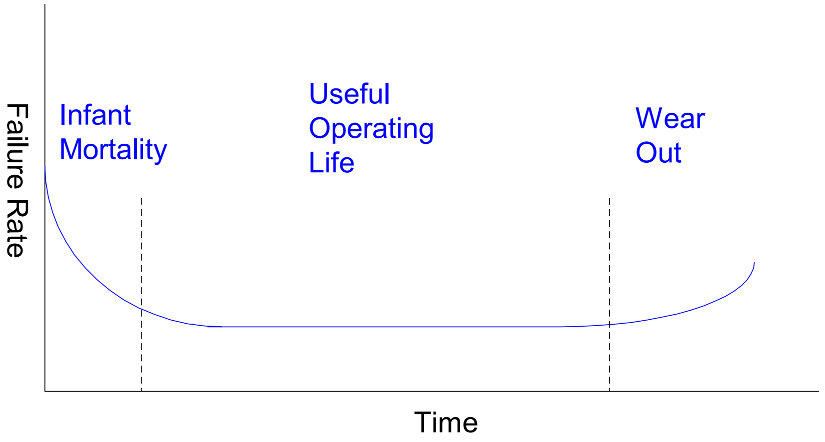


Noise

- Sources
  - Power supply noise / ground bounce
  - Capacitive coupling
  - Charge sharing
  - Leakage
  - Noise feedthrough
- Consequences
  - Increased delay (for noise to settle out)
  - Or incorrect computations

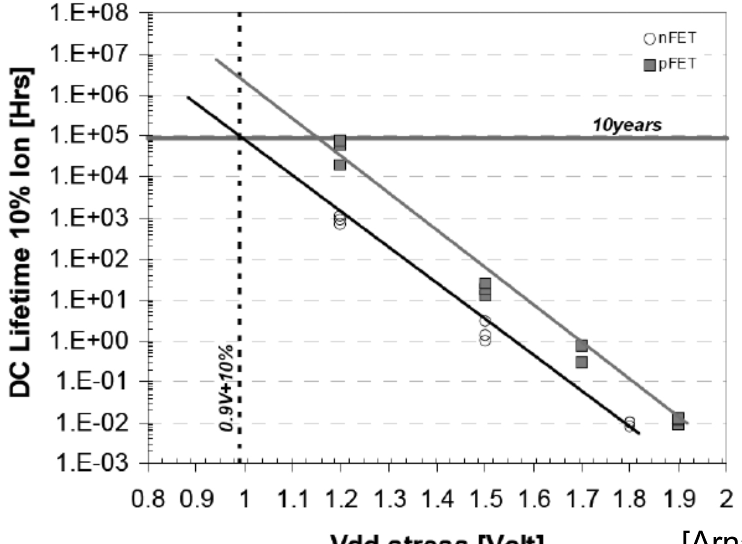
Reliability

- Hard Errors
  - Oxide wearout
  - Interconnect wearout
  - Overvoltage failure
  - Latchup
- Soft Errors
- Characterizing reliability
  - Mean time between failures (MTBF)
    - # of devices x hours of operation / number of failures
  - Failures in time (FIT)
    - # of failures / thousand hours / million devices



Accelerated Lifetime Testing

- Expected reliability typically exceeds 10 years
- But products come to market in 1-2 years
- Accelerated lifetime testing required to predict adequate long-term reliability



[Arnaud08]

Hot Carriers

- Electric fields across channel impart high energies to some carriers
  - These "hot" carriers may be blasted into the gate oxide where they become trapped
  - Accumulation of charge in oxide causes shift in V_t over time
  - Eventually V_t shifts too far for devices to operate correctly
- Choose V_{DD} to achieve reasonable product lifetime
  - Worst problems for inverters and NORs with slow input risetime and long propagation delays

NBTI

- *Negative bias temperature instability*
- Electric field applied across oxide forms dangling bonds called traps at Si-SiO_2 interface
- Accumulation of traps causes V_t shift
- Most pronounced for pMOS transistors with strong negative bias ($V_g = 0$, $V_s = V_{DD}$) at high temperature

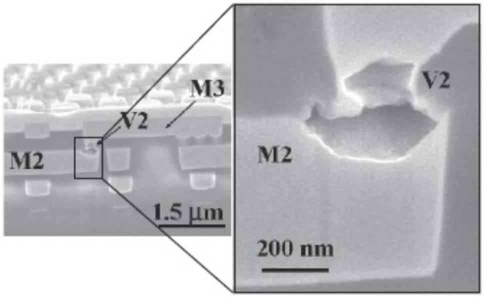
$$\Delta V_t = k e^{\frac{E_{ox}}{E_0}} t^{0.25} \qquad E_{ox} = V_{DD}/t_{ox}$$

TDDB

- *Time-dependent dielectric breakdown*
  - Gradual increase in gate leakage when an electric field is applied across an oxide
  - a.k.a *stress-induced leakage current*
- For 10-year life at 125 C, keep E_{ox} below ~0.7 V/nm

Electromigration

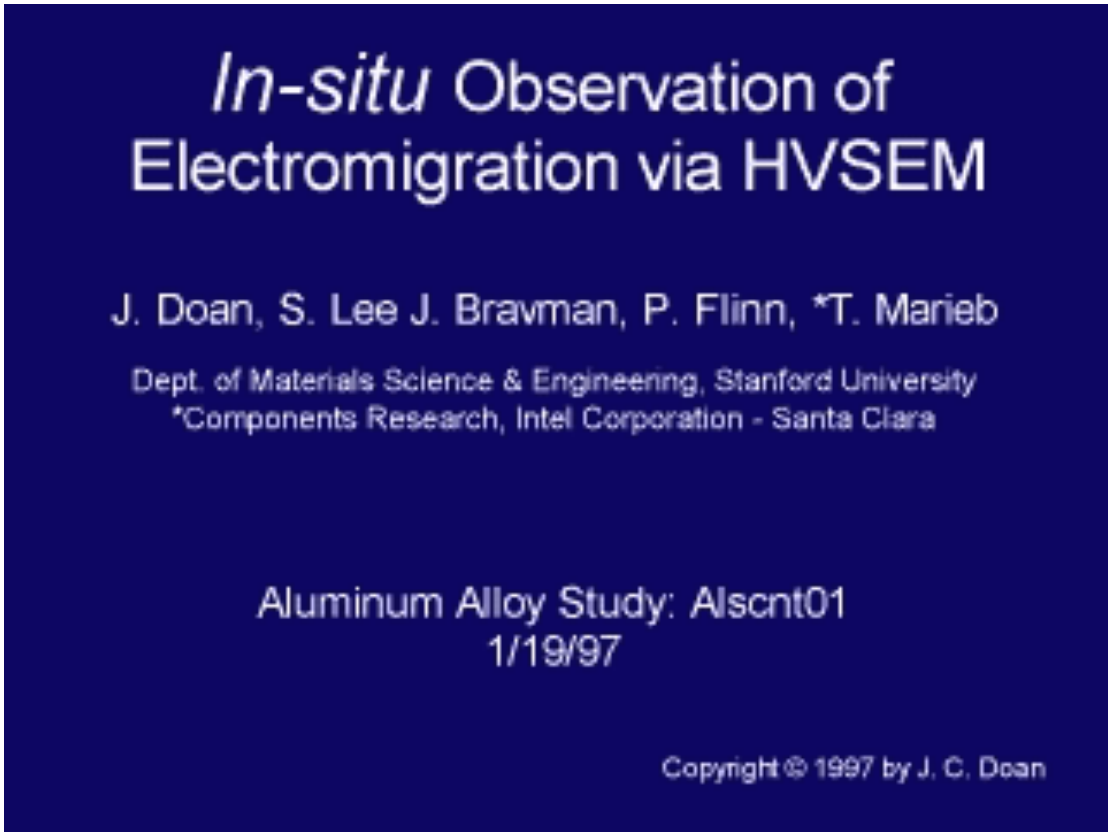
- "Electron wind" causes movement of metal atoms along wires
- Excessive electromigration leads to open circuits
- Most significant for unidirectional (DC) current
  - Depends on current density J_{dc} (current / area)
  - Exponential dependence on temperature
  - Black's Equation: $MTTF \propto \frac{e^{\frac{E_a}{kT}}}{J_{dc}{}^{n}}$
  - Typical limits: $J_{dc} < 1 – 2$ mA / µm^2



[Christiansen06]

Electromigration Video

Electromigration Video 2



Self-Heating

- Current through wire resistance generates heat
  - Oxide surrounding wires is a thermal insulator
  - Heat tends to build up in wires
  - Hotter wires are more resistive, slower
- Self-heating limits AC current densities for reliability

$$I_{rms} = \sqrt{\frac{\int_0^T I(t)^2 \, dt}{T}}$$

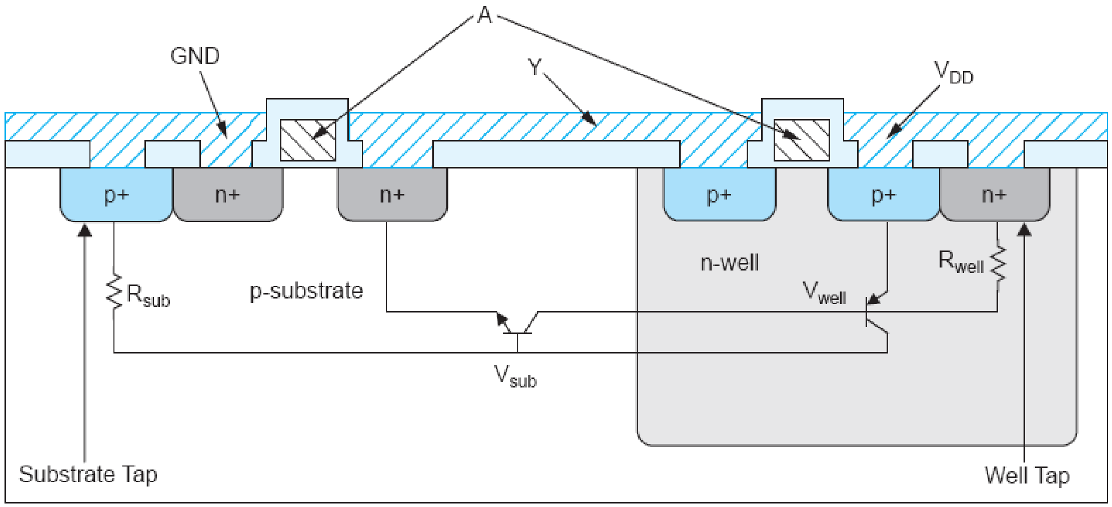
  - Typical limits: $J_{rms} < 15$ mA / μm^2

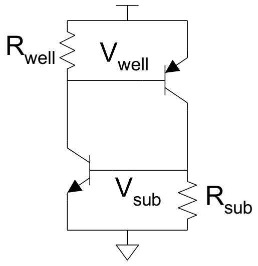
Overvoltage Failure

- High voltages can blow out tiny transistors
- *Electrostatic discharge* (ESD)
  - kilovolts from static electricity when the package pins are handled
- *Oxide breakdown*
  - In a 65 nm process, $V_g \approx 3$ V causes *arcing* through thin gate oxides
- *Punchthrough*
  - High V_{ds} causes depletion region between source and drain to touch, leading to high current flow and destructive overheating

Latchup

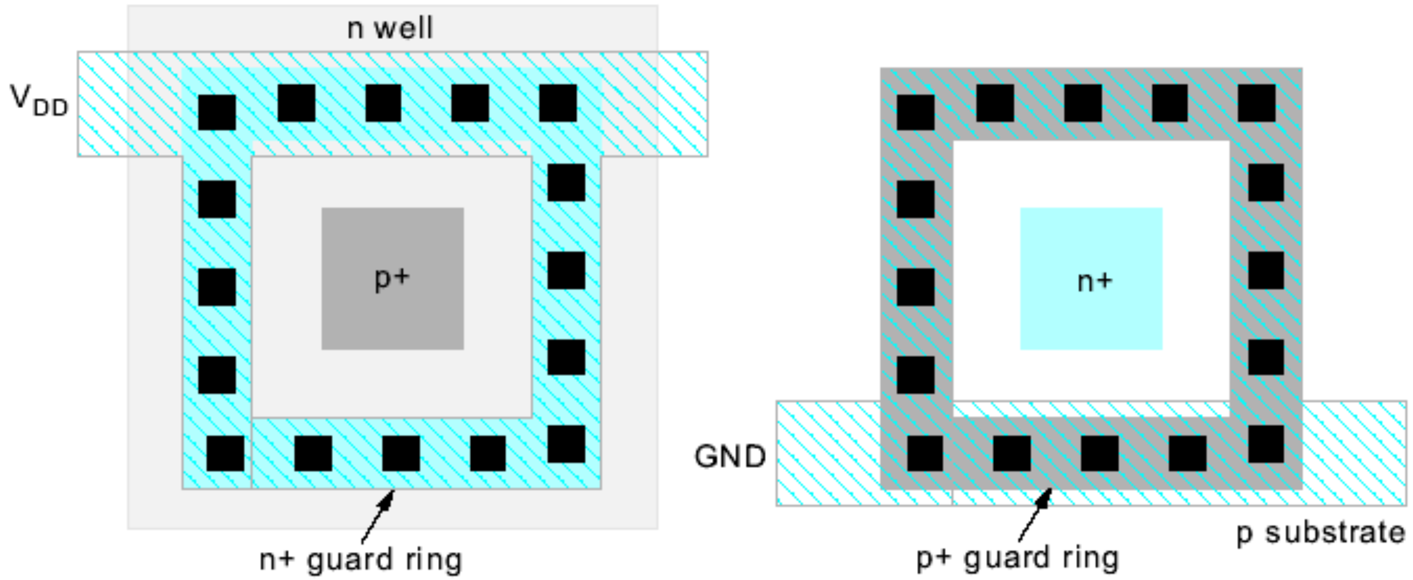
- Latchup: positive feedback leading to V_{DD} – GND short
  - Major problem for 1970's CMOS processes before it was well understood
- Avoid by minimizing resistance of body to GND / V_{DD}
  - Use plenty of substrate and well taps





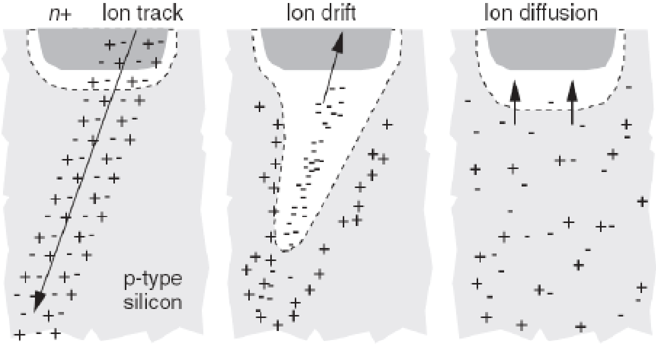
Guard Rings

- Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased
- Surround sensitive region with guard ring to collect injected charge



Soft Errors

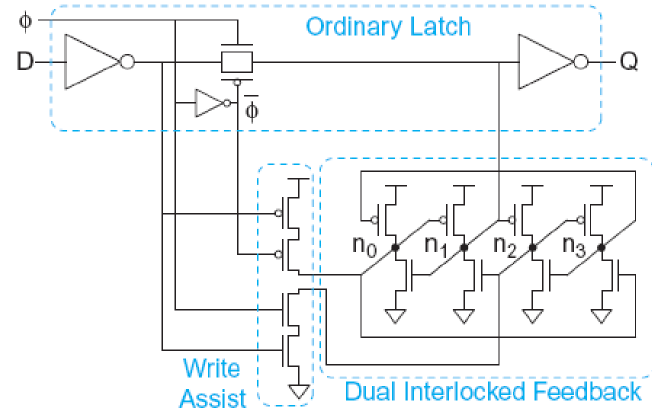
- In 1970's, DRAMs were observed to randomly flip bits
  - Ultimately linked to alpha particles and cosmic ray neutrons
- Collisions with atoms create electron-hole pairs in substrate
  - These carriers are collected on p-n junctions, disturbing the voltage



[Baumann05]

Radiation Hardening

- Radiation hardening reduces soft errors
  - Increase node capacitance to minimize impact of collected charge
  - Or use redundancy
  - E.g. *dual-interlocked cell*



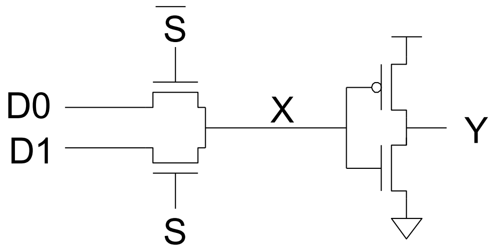
- Error-correcting codes
  - Correct for soft errors that do occur

Circuit Pitfalls

- Detective puzzle
  - Given circuit and symptom, diagnose cause and recommend solution
  - All these pitfalls have caused failures in real chips

Bad Circuit 1

- Circuit
  - 2:1 multiplexer



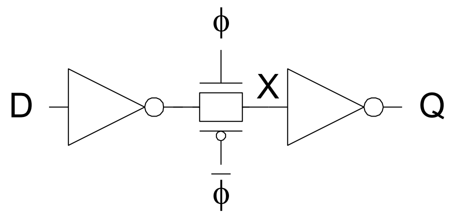
- Principle:
  –
  –
  –

- Solution:

- Symptom
  - Mux works when selected D is 0 but not 1.
  - Or fails at low V_{DD}.
  - Or fails in SFSF corner.

Bad Circuit 2

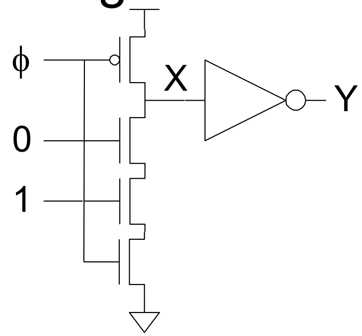
- Circuit
  - Latch



- Symptom
  - Load a 0 into Q
  - Set ϕ = 0
  - Eventually Q spontaneously flips to 1
- Principle:
  -
  -
- Solution:

Bad Circuit 3

- Circuit
  - Domino AND gate

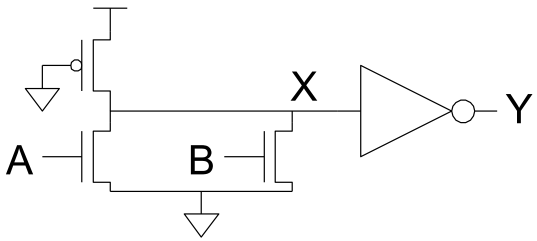


- Principle:
  -
  -
- Solution:

- Symptom
  - Precharge gate (Y=0)
  - Then evaluate
  - Eventually Y spontaneously flips to 1

Bad Circuit 4

- Circuit
  - Pseudo-nMOS OR

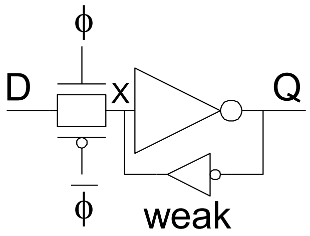


- Principle:
  -
  -
- Solution:

- Symptom
  - When only one input is true, Y = 0.
  - Perhaps only happens in SF corner.

Bad Circuit 5

- Circuit
  - Latch

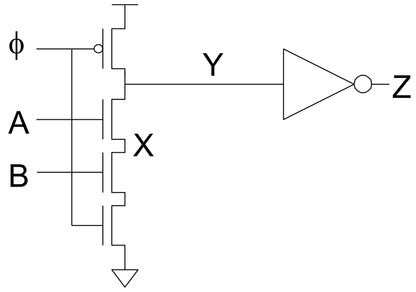


- Principle:
  -
- Solutions:

- Symptom
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

Bad Circuit 6

- Circuit
  - Domino AND gate

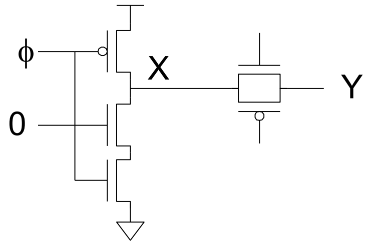


- Principle:
  -
- Solutions:

- Symptom
  - Precharge gate while A = B = 0, so Z = 0
  - Set ϕ = 1
  - A rises
  - Z is observed to sometimes rise

Bad Circuit 7

- Circuit
  - Dynamic gate + latch

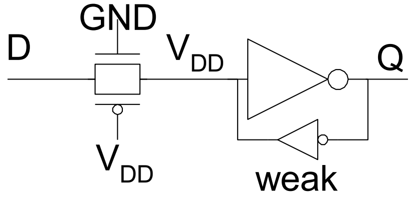


- Principle:
  -
- Solution:

- Symptom
  - Precharge gate while transmission gate latch is opaque
  - Evaluate
  - When latch becomes transparent, X falls

Bad Circuit 8

- Circuit
  - Latch



- Symptom
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver

- Principle:
  -
  -
- Solution:

Summary

- Static CMOS gates are very robust
  - Will settle to correct value if you wait long enough
- Other circuits suffer from a variety of pitfalls
  - Tradeoff between performance & robustness
- Essential to check circuits for pitfalls
  - For large chips, you need an automatic checker.
  - Design rules aren't worth the paper they are printed on unless you back them up with a tool.