Harris

Introduction to CMOS VLSI Design (E158)

Problem Set 6

Eight wacky freshmen designed the Muddle Chip in Fall of 2003. The chip contains a number of logic functions, some of which operate correctly and some of which do not. Even for the circuits with no logic or electrical bugs, some of the chips may not work because of manufacturing problems (e.g. a speck of dust on the wafer).

A TestosterICs chip tester is setup in the VLSI Lab opposite the entrance. The setup includes the Brain Box, 40-pin Device Under Test (DUT) card, a 14-pin 74LS04 inverter chip, a user manual, a Muddle chip report, and two Muddle chips. Learn to use the tester by following the tutorial on pages 7-9 of the TestosterICs user manual.

Documentation for the Muddle Chip, including a chip report (less the sections on intentional errors and testing), the Electric library, and a .dev pinmap file are in C:\testergen\muddle.

Your task is to test one of the circuits on one of the chips. Study the Muddle chip report to understand how the circuit works. Either prove that it operates according to the specification or show that it does not meet specifications and diagnose the source of the error. Use the smallest number of test vectors necessary to prove the circuit has no stuck-at faults. You may have to refer to the layout, schematic, or Electric library for your diagnosis. The specific chip you are responsible for will be assigned in class.

Turn in a 1-page report either explaining how you proved the circuit works or explaining where it fails and why. You may work alone or in a pair with the other person testing the same circuit on the same chip. If you work in a pair, turn in a single report with both of your names on it.