Introduction to CMOS VLSI Design (E158)

Harris

Syllabus

Spring 2010

Teaching Staff

Professor:	David Money Harris	Parsons 2374	x73623	David_Harris@hmc.edu

Schedule

Lecture: MW 11-12:15 Parsons 1285
Office Hours: TBD
Design Reviews: Tuesdays 7:30-10:30 PM after Spring Break

Feel free to stop by even if I do not have official office hours.

Texts

CMOS VLSI Design, 4^{th} Ed., (Weste & Harris, Addison-Wesley, 2010) is the primary text. A draft will be available in a binder before the book goes to press. I will give extra credit to the first person to report a given bug in the book.

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e158
Class email list: eng-158

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-158

Learning Objectives

At the end of this class, you will have designed and validated your own chip. You will understand the impact of design choices on speed, power, reliability, and cost and be able to make appropriate trade-offs, confirming your back-of-the-envelope analysis with simulation. You will be familiar with options for designing interconnect, datapaths, memories, and special-purpose circuits. You will be able to apply modern design methods and industry-standard tools to both custom and synthesized blocks. You will take a complex system from specification through detailed design and verification with a teammate and will provide oral and written reports on your work.

Grading

Labs:	10%
Problem Sets:	15%
In-class Activities:	5%
Project 1:	20%
Project 2:	50%

The emphasis of this class is hands-on chip design. During the first four weeks, you will complete a series of labs to build an 8-bit MIPS microprocessor. Along the way, you will master a variety of CAD tools and design techniques.

Labs and problem sets are due by the end of class and will not be graded if submitted late. However, the labs build toward assembly of the entire processor, so it is important not to fall behind. Your lowest problem set and two activity scores will be dropped before the average is calculated; if you need to miss more classes because of interviews or illness, contact Prof. Harris.

There are two projects this year. The first is to build a 20-bit adder optimized for energy and delay. You will work by yourself on this project to explore designing a subsystem of moderate complexity. The second is to design an entire chip for a purpose of your choosing. You will work with a partner to write a specification and design and validate the chip. If you have a junior on your team who is willing to test the chip and the project is sufficiently validated, you may be able to tape it out and have it fabricated over the summer.

Honor Code Policy

1. All students enrolled in this course are bound by the HMC Honor Code. More information on the HMC Honor Code can be found in the HMC Student Handbook.
2. It is your responsibility to determine whether your actions adhere to the HMC Honor Code. If this document does not clarify the legitimacy of a particular action, you should contact the course instructor and request clarification.
3. Work you submit for individual assignments should be your own, and you should complete all assignments based on your own understanding of the underlying material. If you work with, or receive help from, another individual on an assignment, provide a written acknowledgement in complete sentences that includes the person's name and the nature of the help.
4. This document is not meant to be an exhaustive list of every possible Honor Code violation. Infractions not explicitly mentioned here may still violate the Honor Code.
5. Boundaries of Collaboration

   Verbal collaboration with other students on individual assignments is encouraged AFTER you have given serious thought to each component yourself. However, all submitted written work should be written by yourself individually, and not a collaborative effort or copied from a common source (e.g., a chalkboard). It is NOT acceptable to work on labs in lockstep with another classmate.
6. Use of Published Solutions

   You may check your answers against the solutions in the back of the textbook after completing problems, but may not reference step-by-step solution instructions in separately published solution manuals.
7. Use of Computer Software

   The use of graphing calculators and computer software to aid in course work is acceptable, as long as it does not substitute for an understanding of the course material.
8. Use of Web Resources

   The use of Internet resources to aid in course work is acceptable, as long it does not substitute for an understanding of the course material. Plagiarism and direct copying from online (or any other) sources is strictly prohibited. You may NOT refer to solutions to textbook problems floating around on the Web.
9. Use of Your Own Work from Previous Semesters

   If you have previously attempted this course, you may resubmit your work from previous semesters as this semester's coursework, as long as you understand the underlying material.
10. Use of Other Course Resources from Previous Semesters

    You may reference the tests of this course from previous semesters as study aids. You may not reference assignments (labs, problem sets, activities) of this course from previous semesters.
11. Retention of Course Resources

    Assignments and exams from this course may be committed to dorm repositories or otherwise used to help future students.

Tentative Schedule

The attached schedule is a tentative plan that may change during the semester. The schedule lists reading associated with each lecture. You are expected to do the reading before class and be prepared to discuss it. However, you may skip over optional section.

00000	20-Jan	Introduction and overview		
00001	25-Jan	Circuits and layout	1.1-1.5	
00010	27-Jan	Design flow	1.6-1.12	Lab 1: Cell Design
00011	1-Feb	CMOS transistor theory	2.1-2.3	PS 1: Schematics & Sticks
00100	3-Feb	Non-ideal transistor characteristics	2.4	Lab 2: Datapath Design
	8-Feb	-- Silicon Run Video --		
00101	10-Feb	DC & Transient Response	2.5, 4.1-4.3	Lab 3: Control Synthesis
00110	15-Feb	Logical Effort	4.4-4.5	PS 2: Transistors
00111	17-Feb	Power	5.1-5.3	Lab 4: Chip Assembly
01000	22-Feb	Simulation	8.1-8.3, 8.5	PS 3: Logical Effort
01001	24-Feb	Combinational circuit design	9.1	PS 4: Power
01010	1-Mar	Circuit families	9.2	Proj 1 Schematics
01011	3-Mar	Sequential circuit design	10.1-10.3	PS 5: SPICE
01100	8-Mar	Design for testability	15.6	Proj 2 Proposal
01101	10-Mar	Adder Presentations		Proj 1 Optimization
	15-Mar	-- Spring Break: No Class --		
	17-Mar	-- Spring Break: No Class --		
01110	22-Mar	Wires	6.1-6.4	Proj 2 Verilog
01111	24-Mar	Ivan Sutherland Guest Lecture: Proximity Comm.		
10000	29-Mar	Scaling and variability	7.1-7.2, 7.4	Proj 2 Schematics
10001	31-Mar	Circuit pitfalls and reliability	9.3, 7.3	
10010	5-Apr	Adders	11.1-11.2	Proj 2 Block Layouts
10011	7-Apr	Datapath circuit design	11.3-11.9	
10100	12-Apr	Arrays: SRAM	12.1-12.2.3	Proj 2 Chip Layout
10101	14-Apr	Arrays: ROMs, CAMs, PLAs	12.4, 12.6-7	
10110	19-Apr	Packaging, power & clock distribution	13.1-13.4	Proj 2 Final Report
10111	21-Apr	PLLs and DLLs	13.5	
11000	26-Apr	I/O	13.6-13.7	PS 6: Chip testing
11001	28-Apr	Microprocessor Hall of Fame	7.8	

Note: Final project presentations will take place during presentation days (Wednesday May 5).