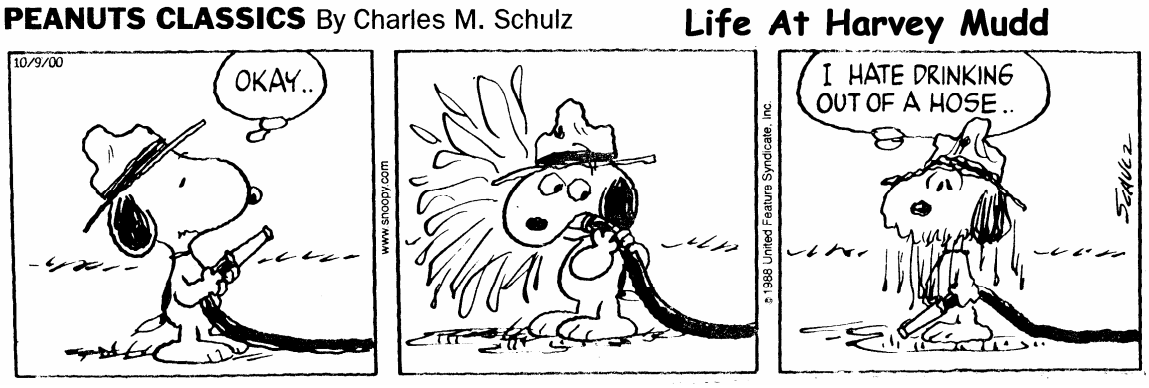
Harris

Introduction to CMOS VLSI Design (E158)

Problem Set 3



1) Logical Effort of a Gate

Consider the AOI gate from Problem Set 1. What are the transistor widths that achieve worst-case rise and fall resistance equivalent to a unit inverter? What is the logical effort of each input (hint: they are not all the same)?

2) Path Delay

Do Exercise 4.13 from the textbook.

3) Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for the future.