MUDDLE

Chip Report

David Harris

December 6, 2003

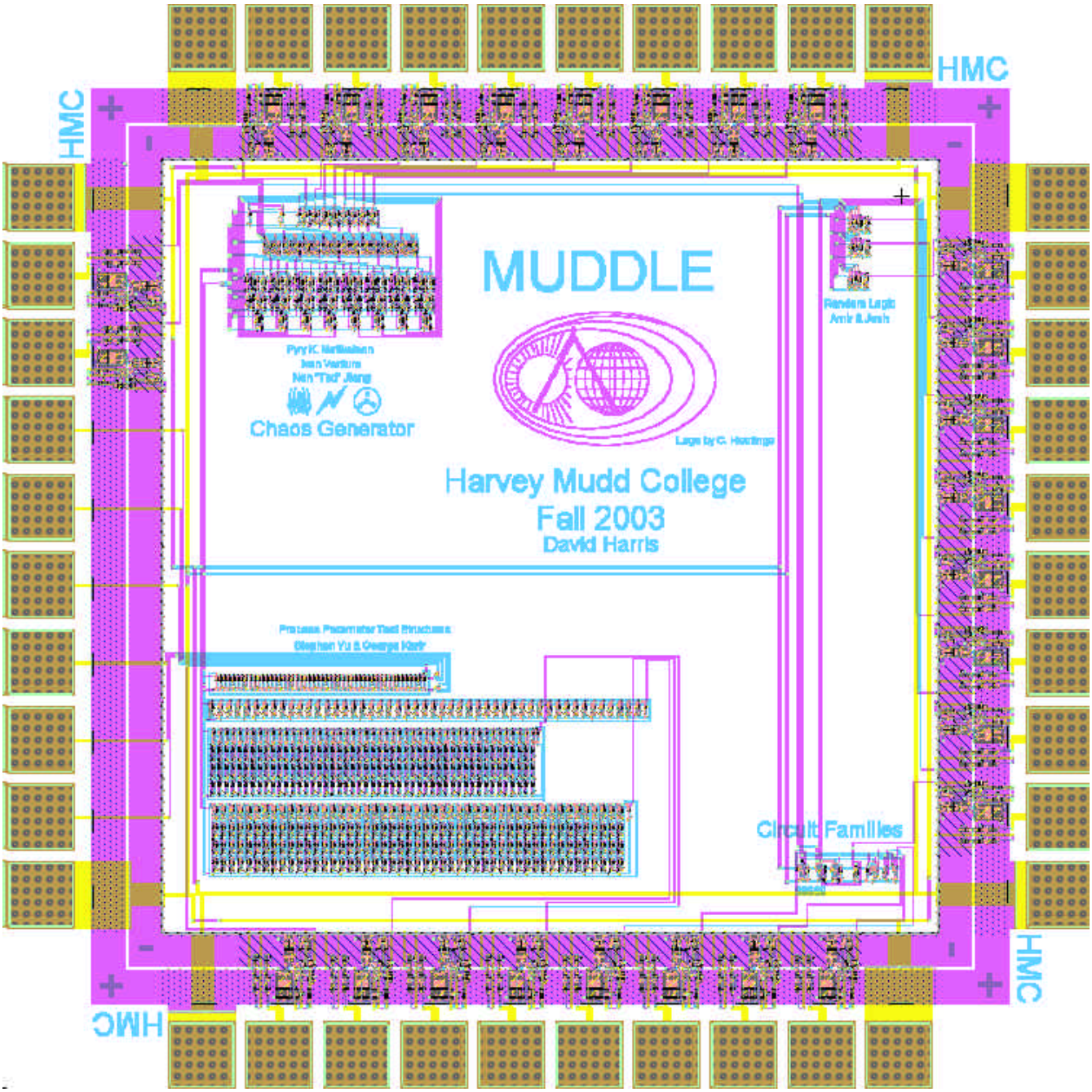


Table of Contents

Introduction

The 2003 Freshman Digital Electronics and Chip Design seminar has designed and built a test chip named MUDDLE. The chip contains a number of logic circuits, some of which are functional and some of which are not. The circuits are intended to serve as a teaching tool to illustrate hardware test and debug for VLSI courses.

The test chip is implemented on a MOSIS 1.5x1.5 mm TinyChip in the AMI 0.5 micron process ($\lambda = 0.3$) in a 40-pin DIP package. It was developed using the Electric CAD suite.

The chip was designed by Amir Adibi, Fang-Yuan Chang, Ted Jiang, Cary Kawamoto, Pyry Matikainen, Joshua Utter-Leyton, Ivan Ventura, and Stephen Yu with George Koirr as lab assistant.

Specifications

MUDDLE has the following inputs and outputs:

Inputs	Outputs
reset	Chaos7…Chaos0
phi1, phi2	InvRing, NandRing, Inv4xRing, Nand4xRing
NMOSG, PMOSG	NMOSS, NMOSD, PMOSS, PMOSD
A, B, C, D	DynamicInv, DynamicNand, DynamicNor, PseudoInv, DominoAnd
	Rand1, Rand2, Rand3

The chip also has 4 VDD pins and 4 GND pins.

MUDDLE has four major units: the Chaos Generator, the Process Parameter Structures, the Circuit Families, and the Random Logic circuits. Each is described further below.

Note that this section describes specification of how the chip ought to function if they had no errors. Errors were introduced into some of the units. These errors will be described in the Actual Operation section..

Chaos Generator

(Pyry, Ted, and Ivan)

The Chaos Generator accepts a reset signal and two-phase nonoverlapping clock. It produces eight Chaos outputs intended to drive LEDs. The outputs will initialize to a known state on reset, the follow a chaotic pattern on each clock cycle.

The Chaos Generator may be viewed as a finite state automata. On reset, Chaos2-4 is initialized high and the others are initialized low. On each subsequent cycle, each output depends on its previous value and the values of its two neighbors according to the following rule

Chaos[i-1]	Chaos[i]	Chaos[i+1]	New Chaos[i]
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Thus the Chaos Generator should trace out the following pattern:

Step	Chaos[0]	Chaos[1]	Chaos[2]	Chaos[3]	Chaos[4]	Chaos[5]	Chaos[6]	Chaos[7]
1	0	0	1	1	1	0	0	0
2	0	1	1	0	0	1	0	0
3	1	1	0	1	1	1	1	0
4	1	0	0	1	0	0	0	0
5	1	1	1	1	1	0	0	1
6	0	0	0	0	0	1	1	1
7	1	0	0	0	1	1	0	0

Random Logic

(Amir & Josh)

The circuit is supposed to compute the following logic table ($\bar{A}BC\bar{D}$):

A	B	C	D	Rand1, 2, 3
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

There are three copies of the circuit. Some of the copies may be good, while others may be bad.

Circuit Families

(Fang-Yuan and Cary)

The circuit consists of five gates GATE that takes input INPUT and gives output OUTPUT as follows:

GATE	INPUT	OUTPUT
Dynamic NAND	A, B, phi	DynamicNand
Dynamic NOR	A, B, phi	DynamicNor
Dynamic Inverter	A, phi	DynamicInv
Domino AND4	A, B, C, D, phi	DominoAnd
Pseudo-nMOS Inverter	A	PseudoInv

Phi comes from the Phi1 input to the chip.

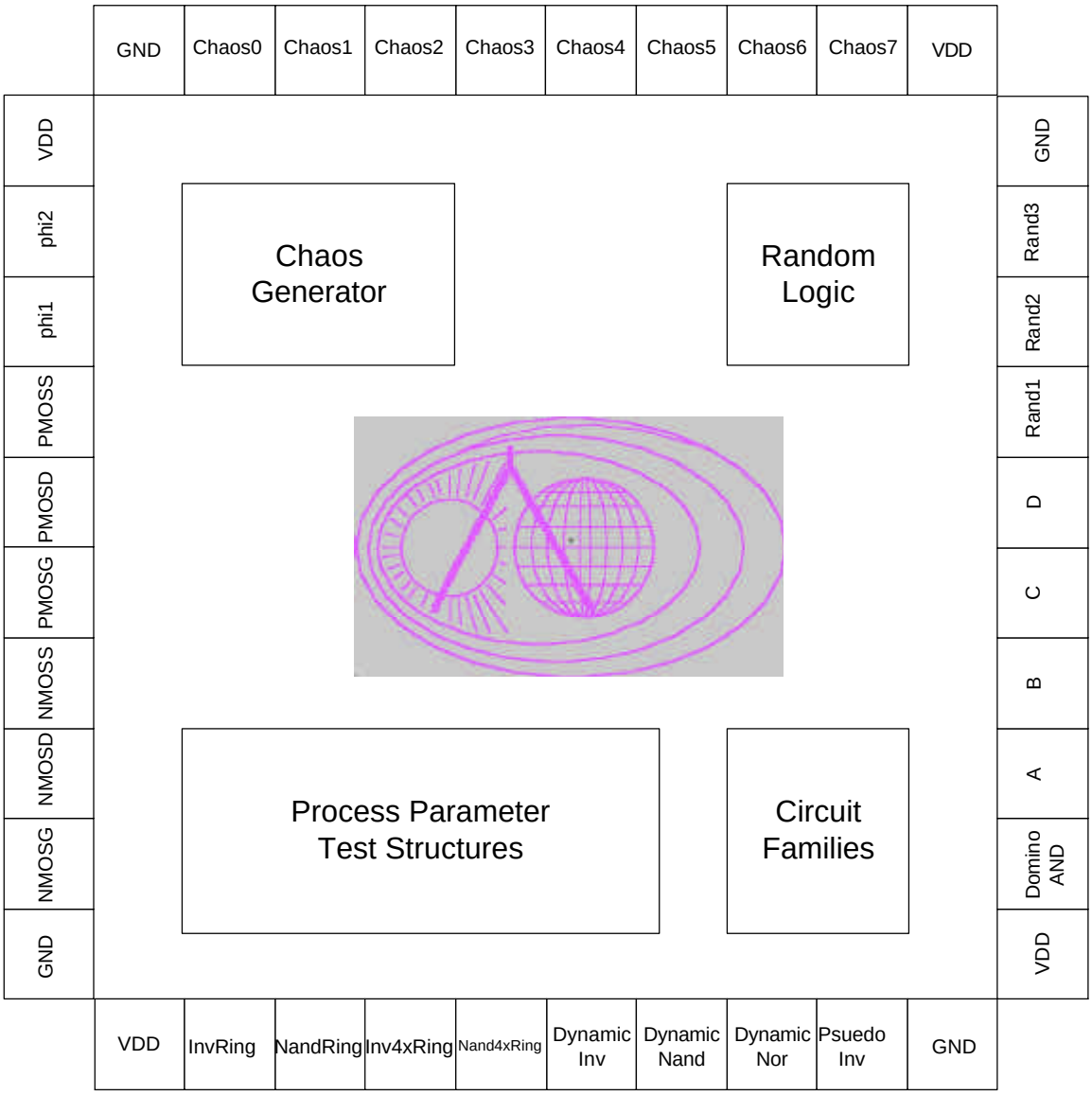
Process Parameter Test Structures

(George and Stephen)

This portion of the chip contains four 49-stage ring oscillators. The oscillators are made of fanout-of-1 and fanout-of-4 inverters and NAND gates. The output of the oscillators is buffered and drives a pin off chip. By measuring the frequencies of the oscillators, one should be able to deduce τ, p_{inv}, and the logical effort and parasitic delay of a NAND gate.

It also contains 12-λ wide nMOS and pMOS transistors. The substrate and well are tied to GND and VDD, respectively. The source, drain, and gate of each transistor are tapped out to analog pads to measure transistor I-V characteristics.

Pinout Diagram



Summary of Files

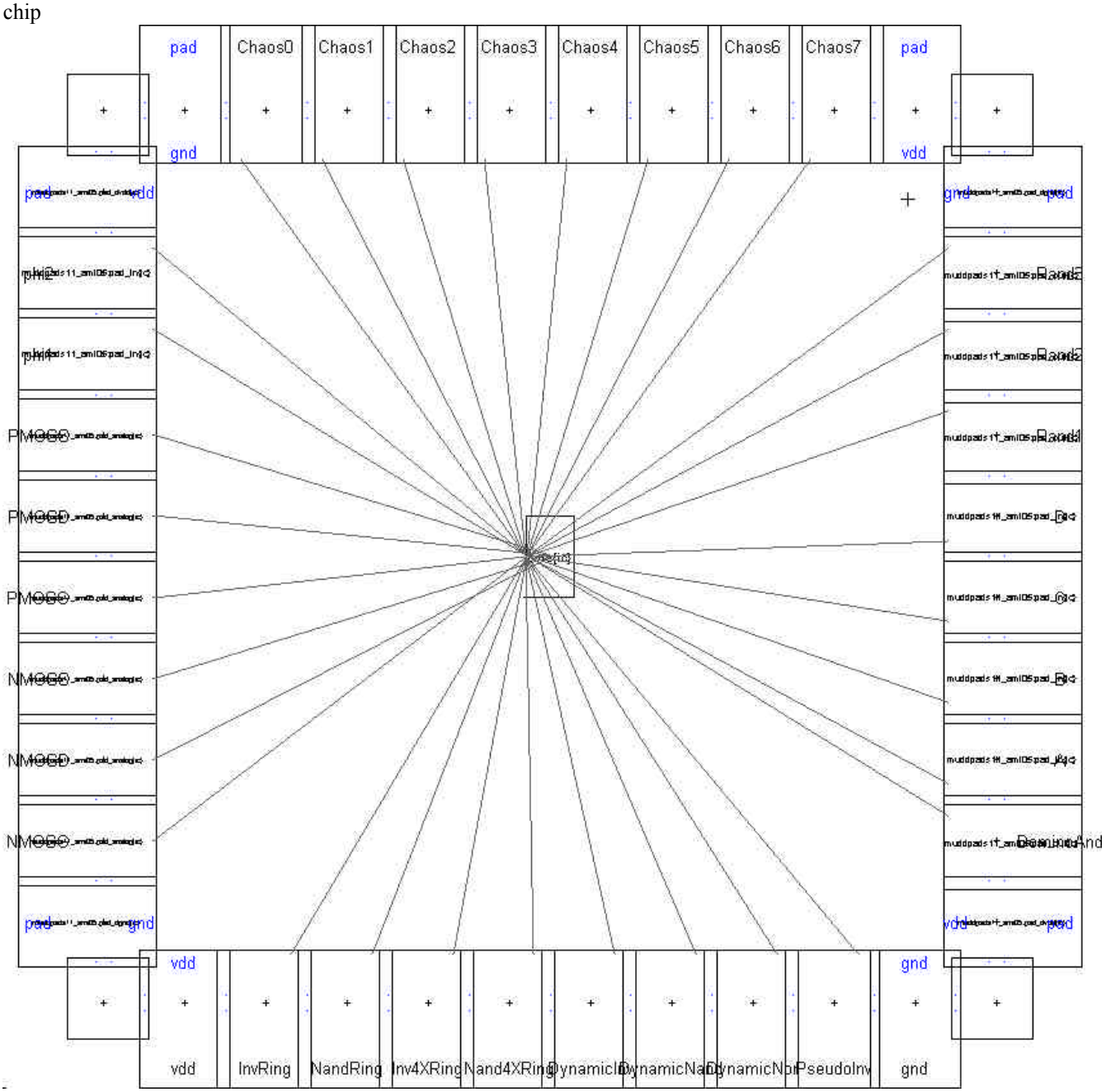
The master files needed to recreate the project are \\Charlie\Courses\Engineering\E158\fys1\MuddleFinal

They include:

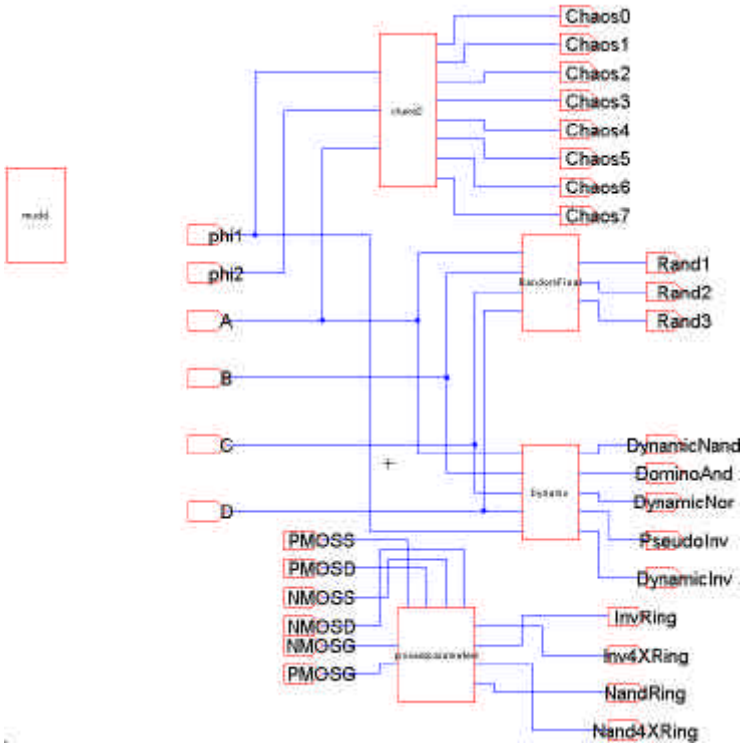
muddle.elib:	the top-level design
muddpads_ami05.elib:	pad frame with HMC logo
chip.cif:	master CIF file
muddle.cmd:	IRSIM command file to test qbert
muddle.arr:	pad arrangement file for layout
muddle.arr	pad arrangement file for schematic

Schematics

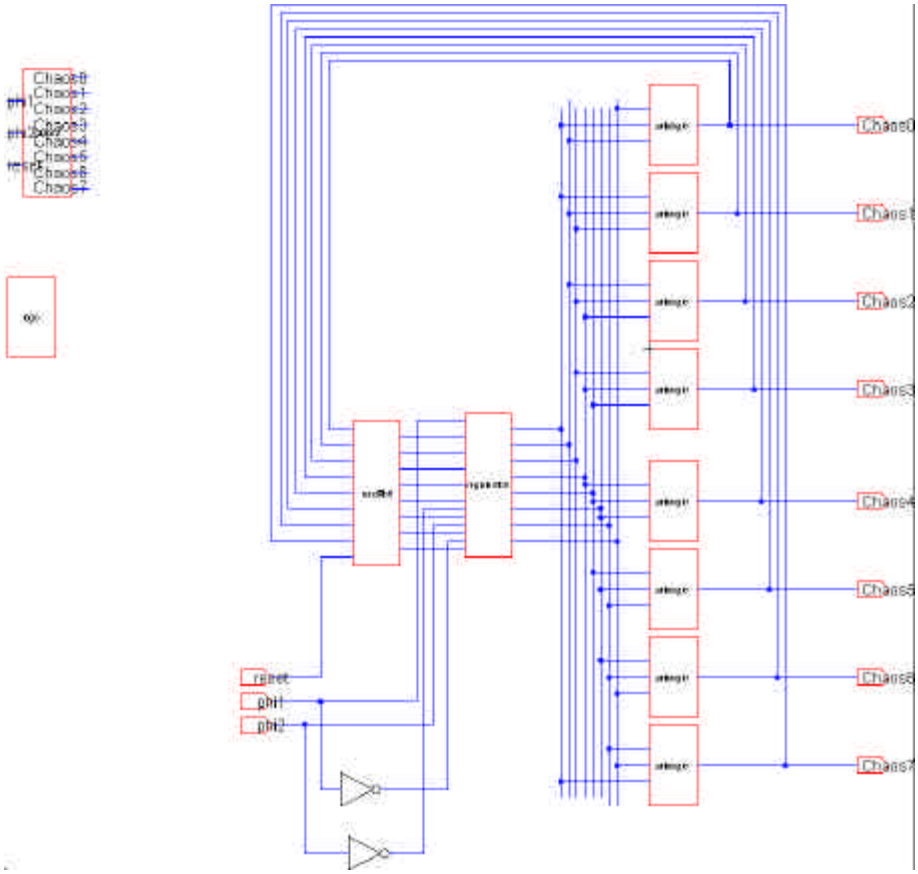
chip



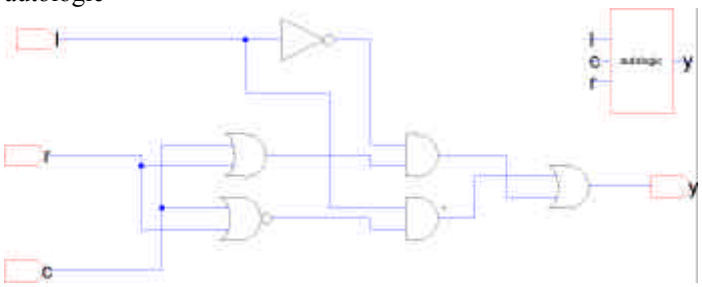
core


Chaos0
Chaos1
Chaos2
Chaos3
Chaos4
Chaos5
Chaos6
Chaos7
phi1
phi2
A
B
C
D
Rand1
Rand2
Rand3
DynamicNand
DominoAnd
DynamicNor
PseudoInv
DynamicInv
PMOSS
PMOSD
NMOSS
NMOSD
NMOSG
PMOSG
InvRing
Inv4XRing
NandRing
Nand4XRing

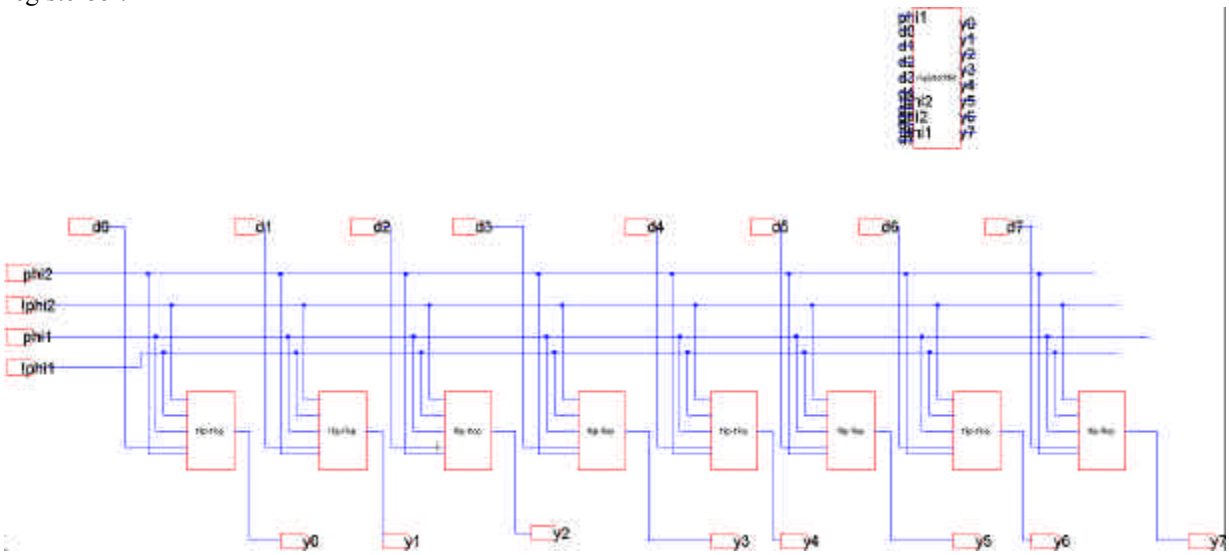
chaos2


Chaos0
Chaos1
Chaos2
Chaos3
Chaos4
Chaos5
Chaos6
Chaos7
reset
phi1
phi2

autologic



register8bit



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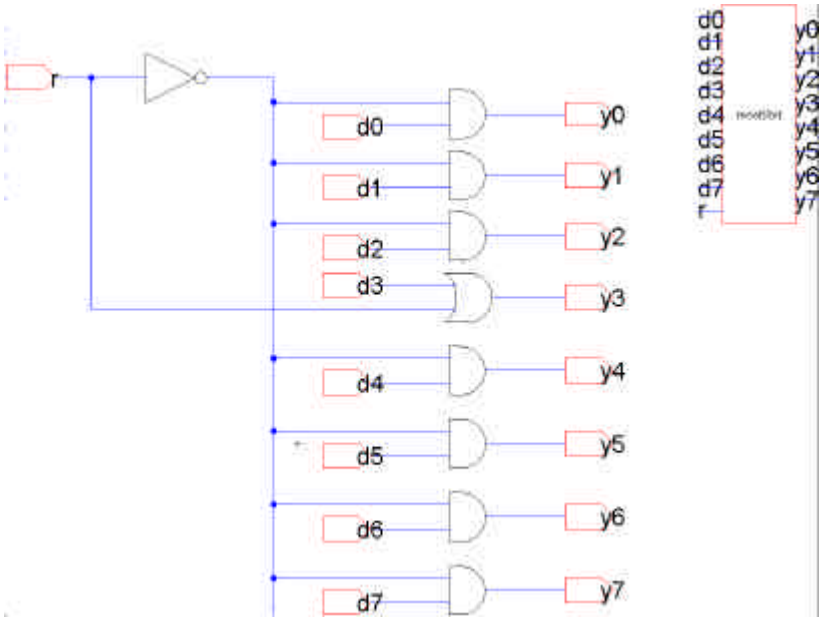

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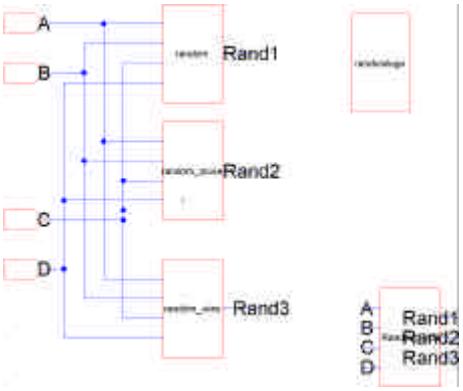

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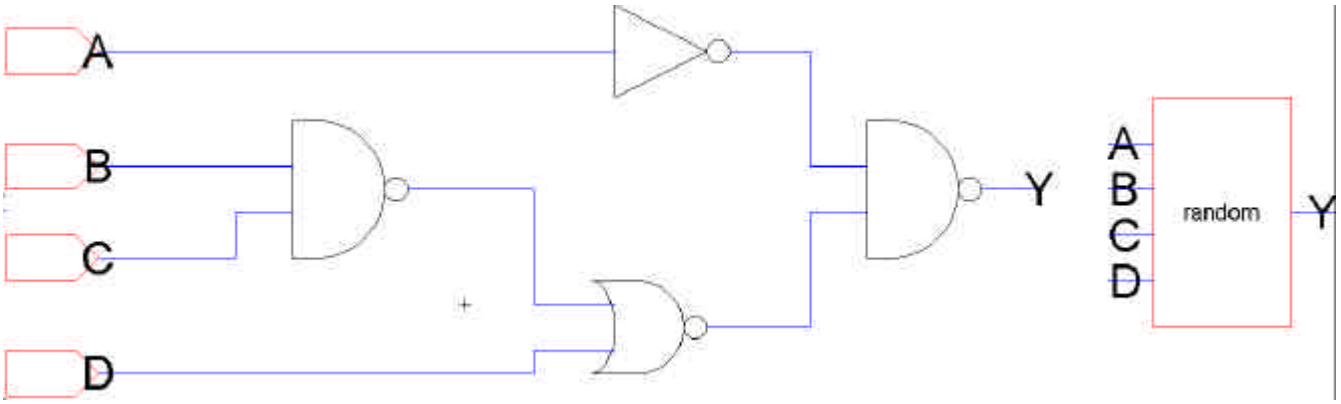

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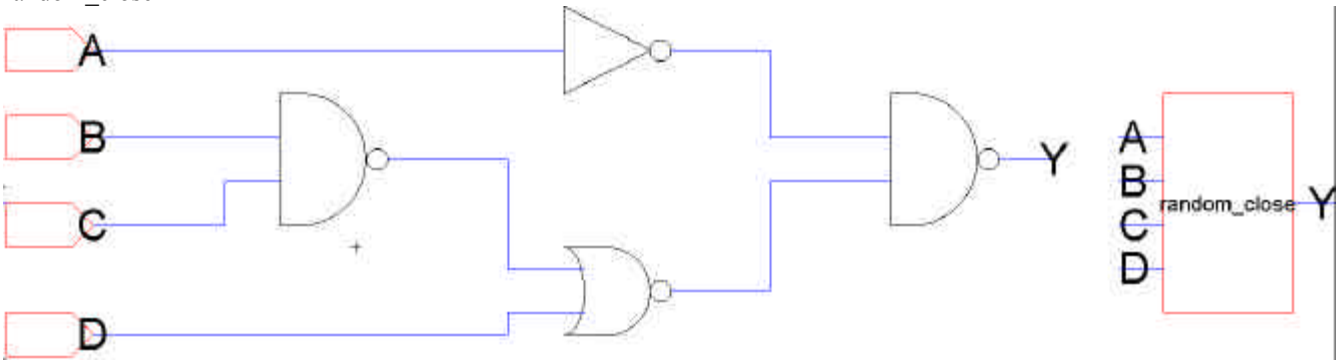

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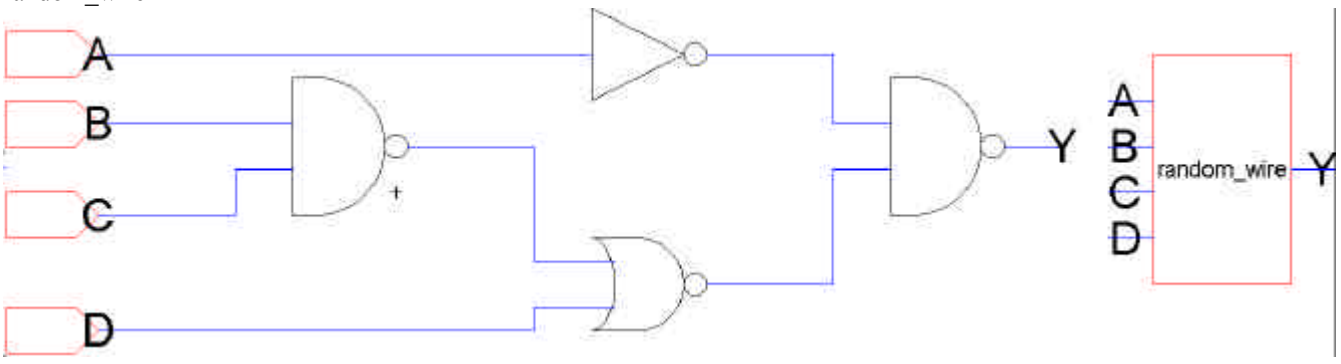
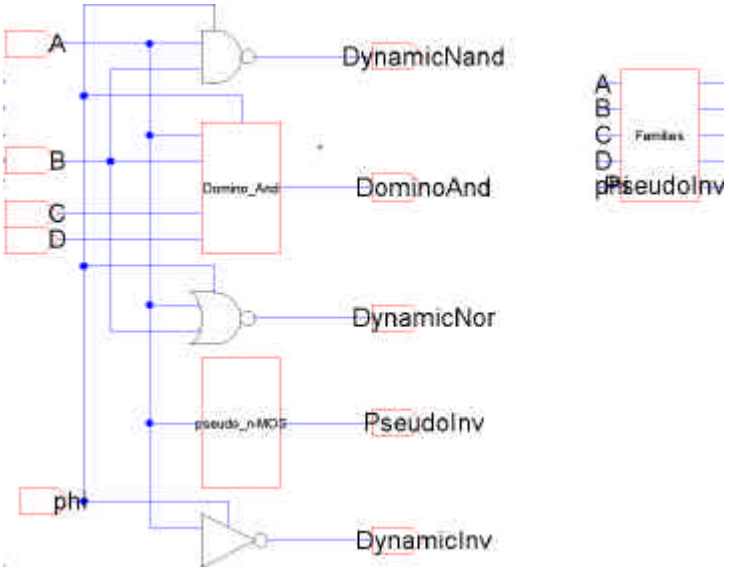


Families



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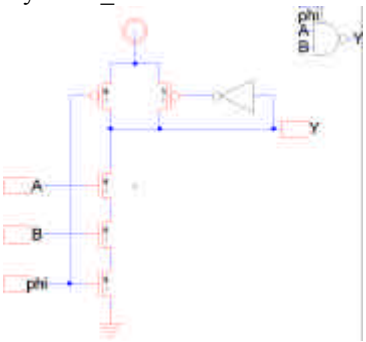
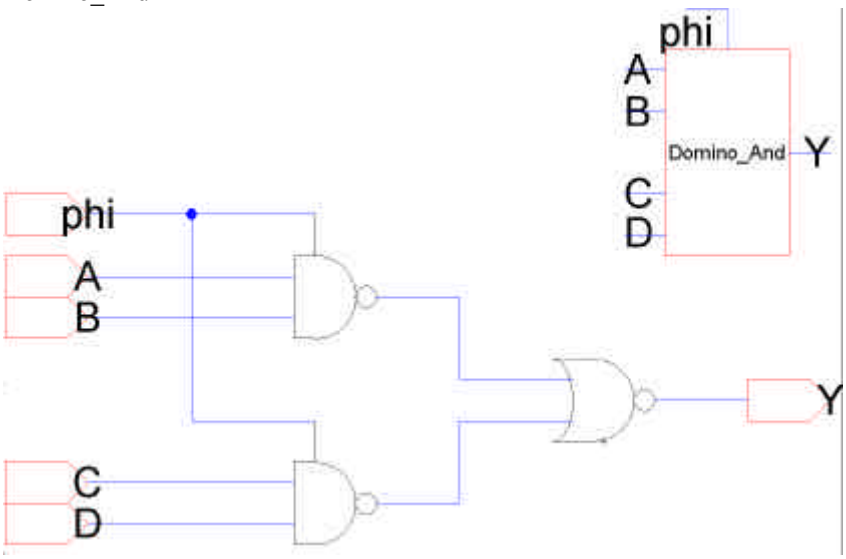


Domino_And



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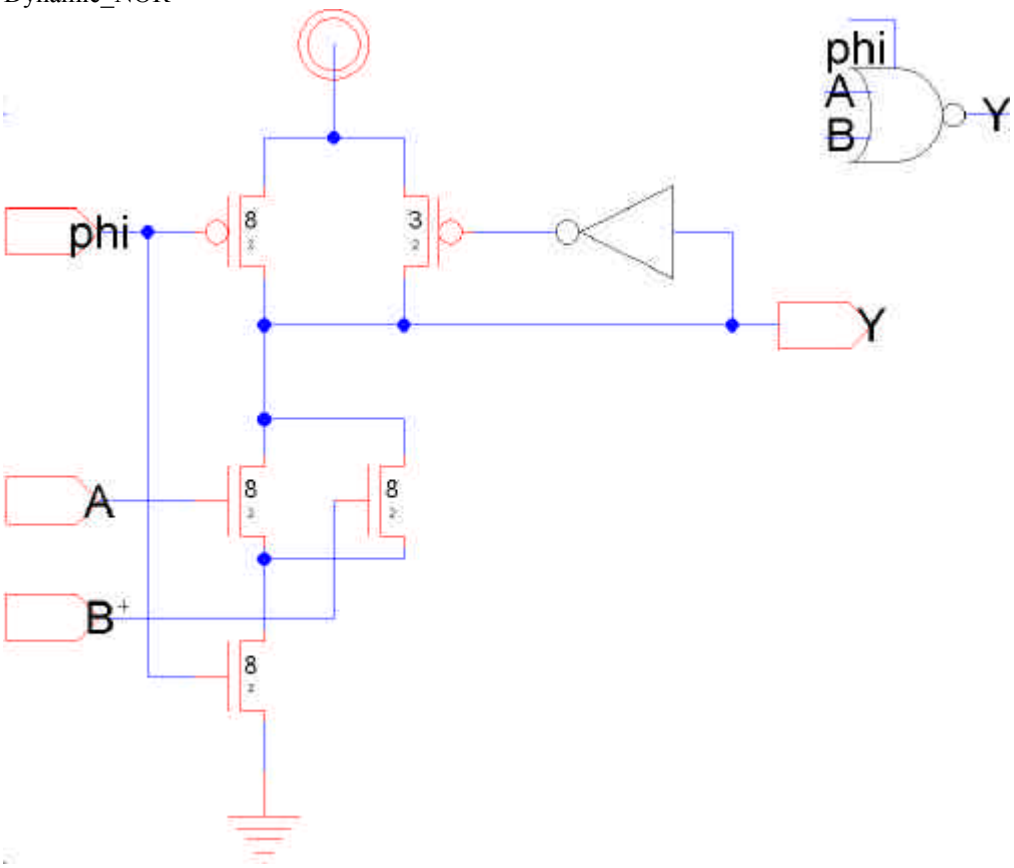

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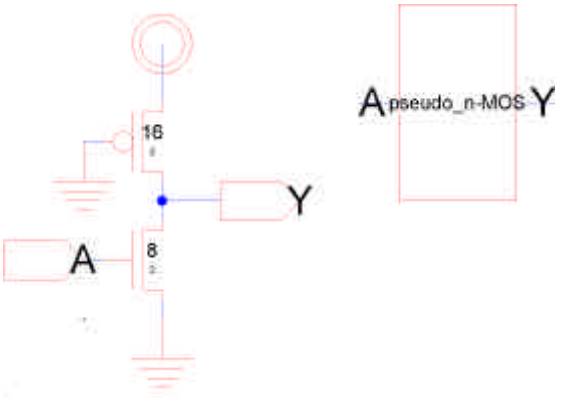

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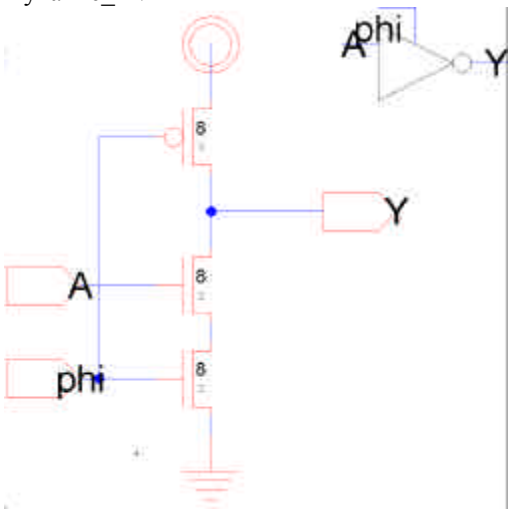

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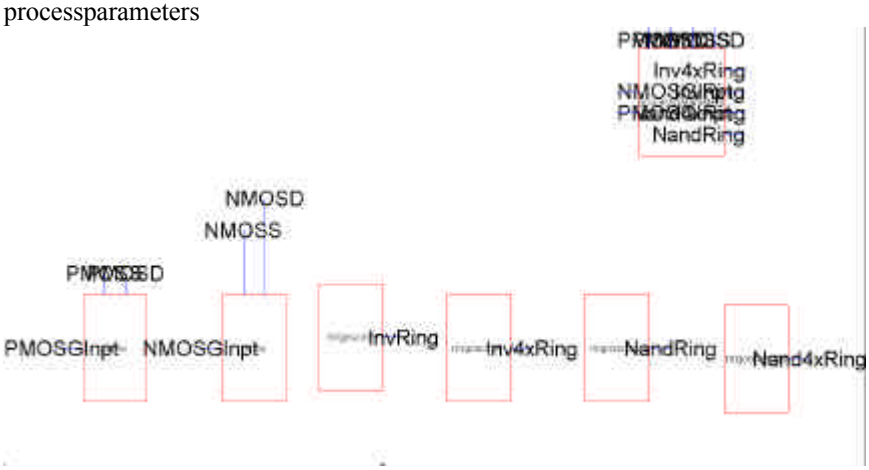

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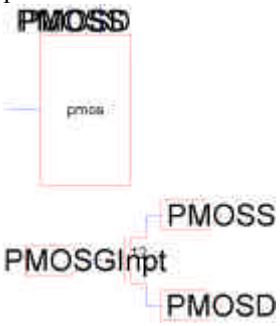

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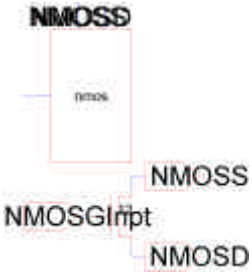
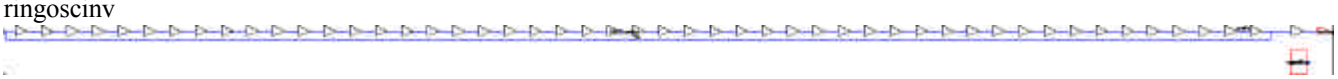
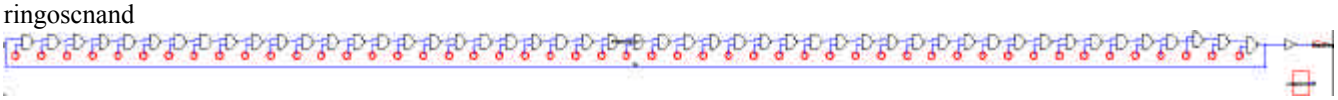


ringoscinv



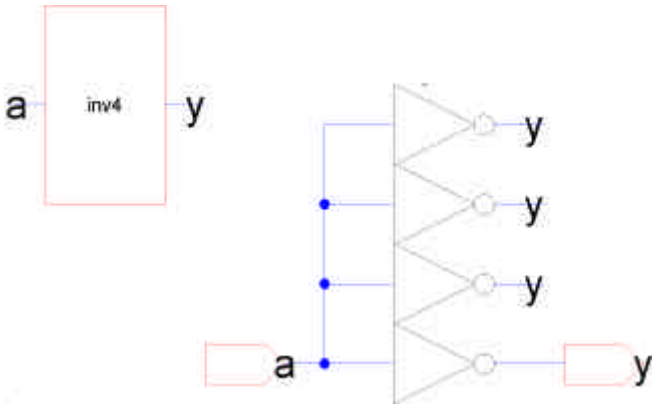
ringoscnand



ringoscinv4

ringoscnand4

inv4



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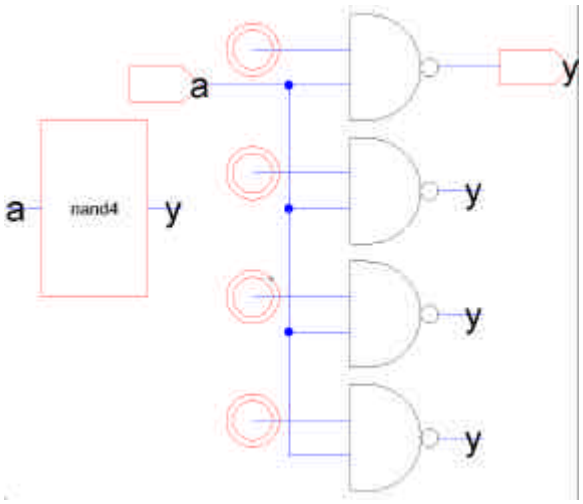
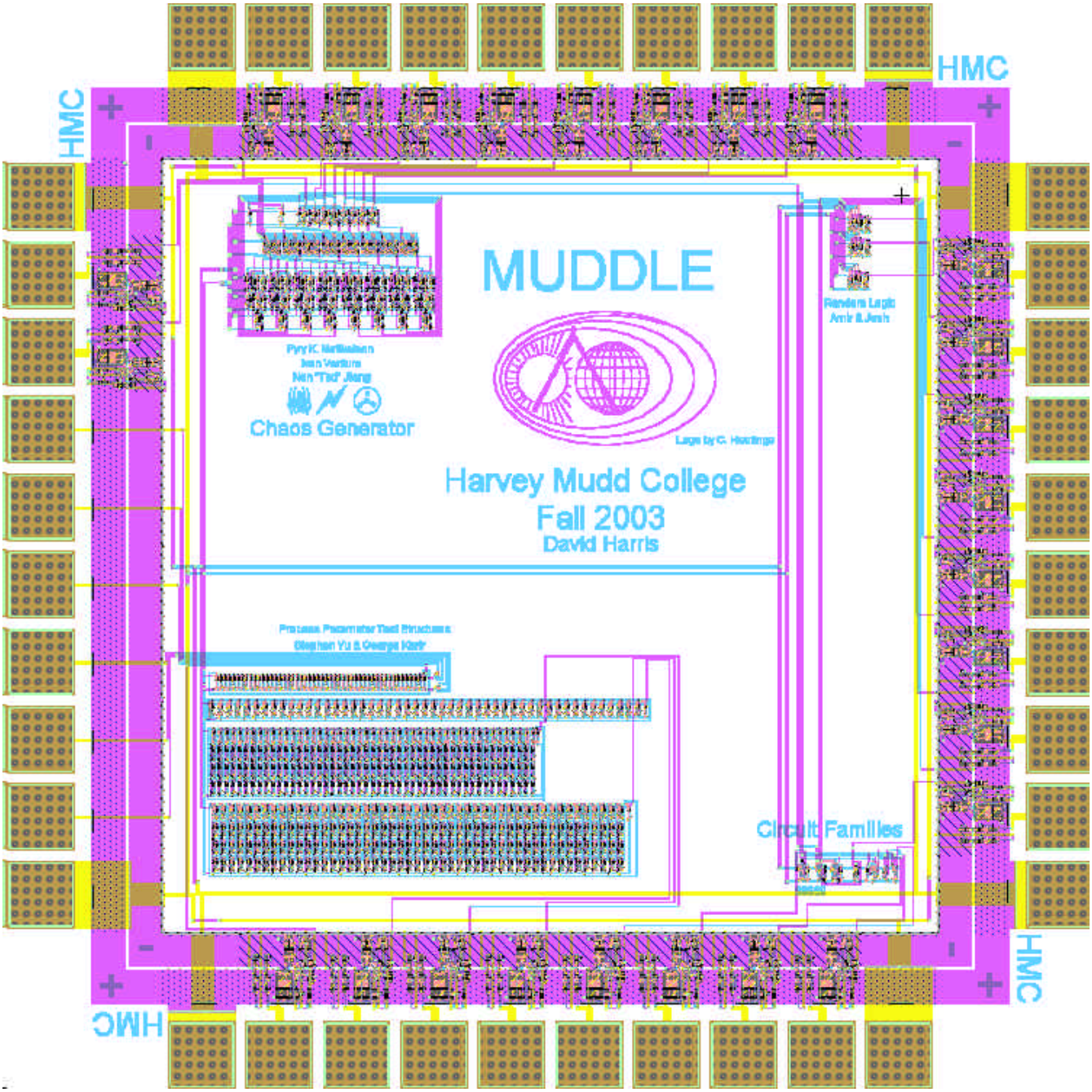


Layout

muddle



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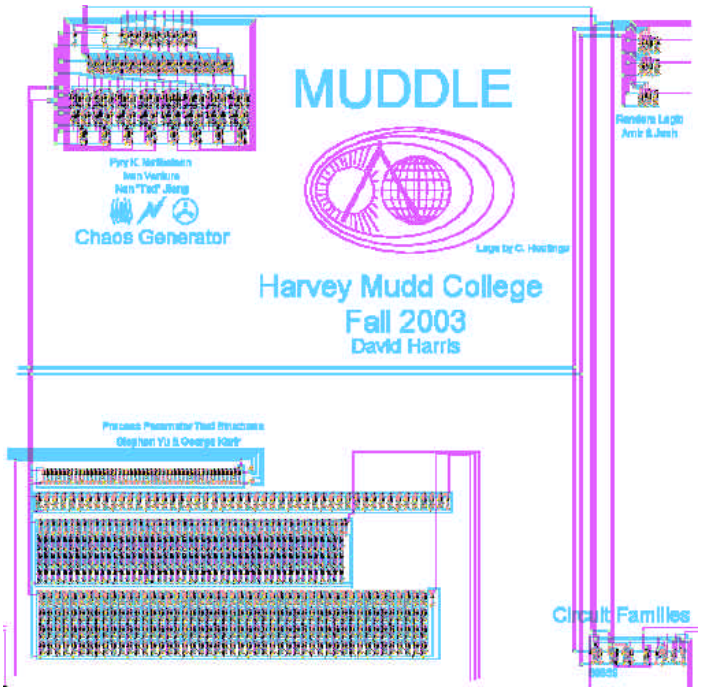
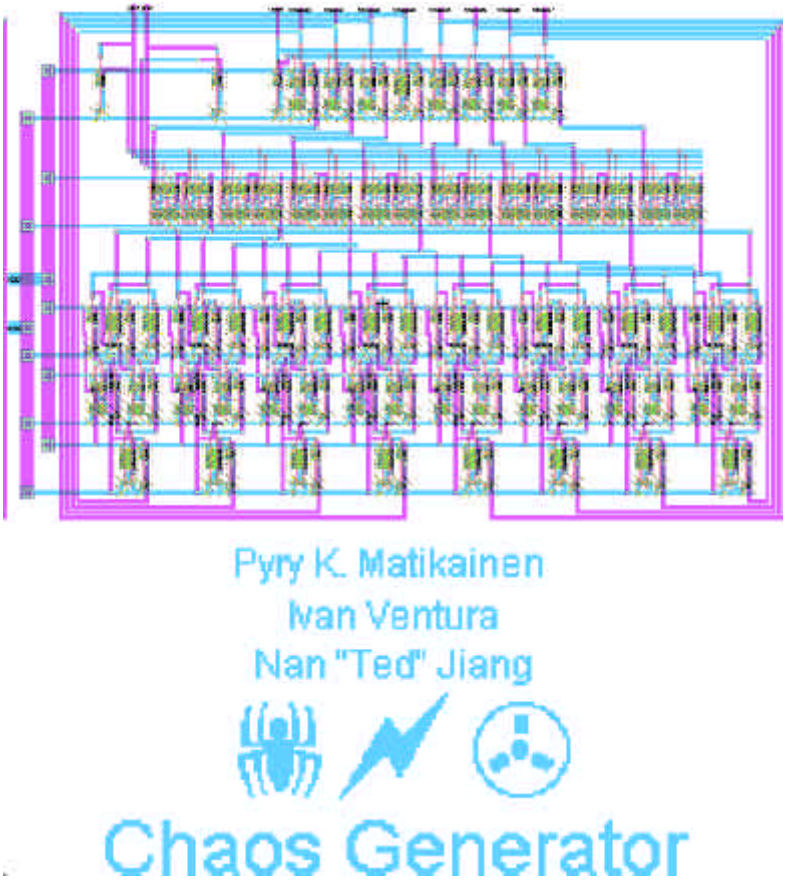
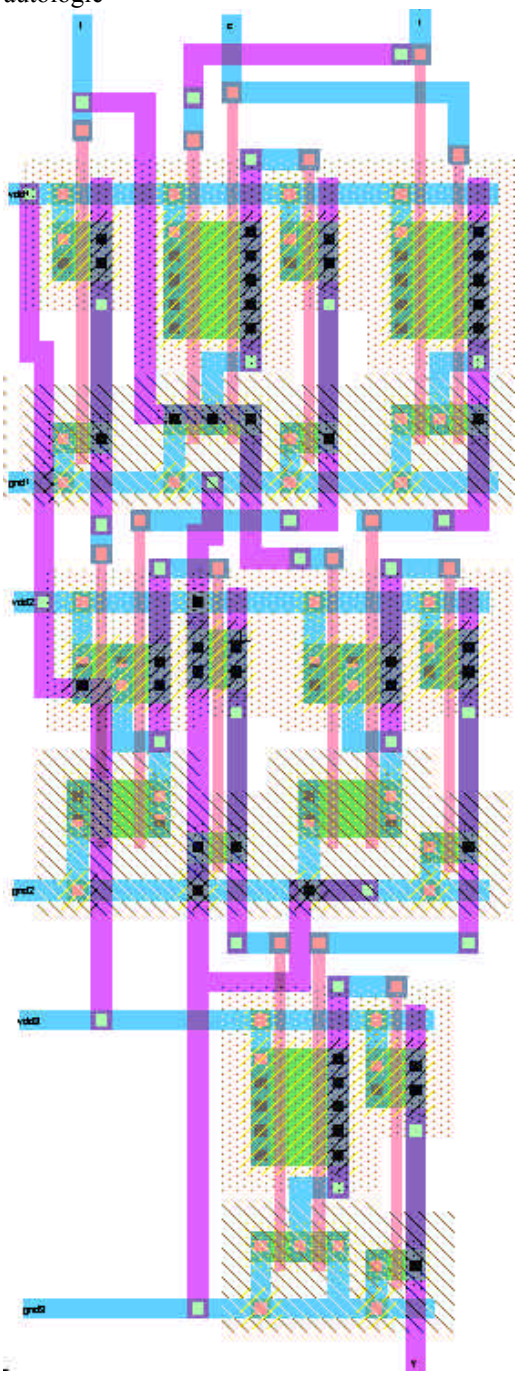

MUDDLE
Chaos Generator
Harvey Mudd College
Fall 2003
David Harris
Circuit Families

chaos2


Pyry K. Matikainen
Ivan Ventura
Nan "Ted" Jiang
Chaos Generator

autologic



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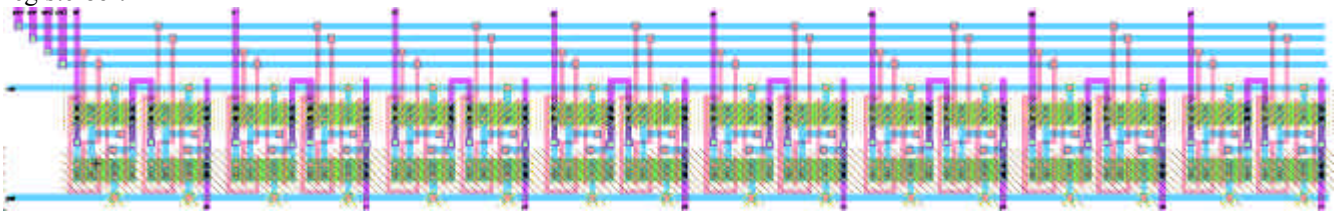

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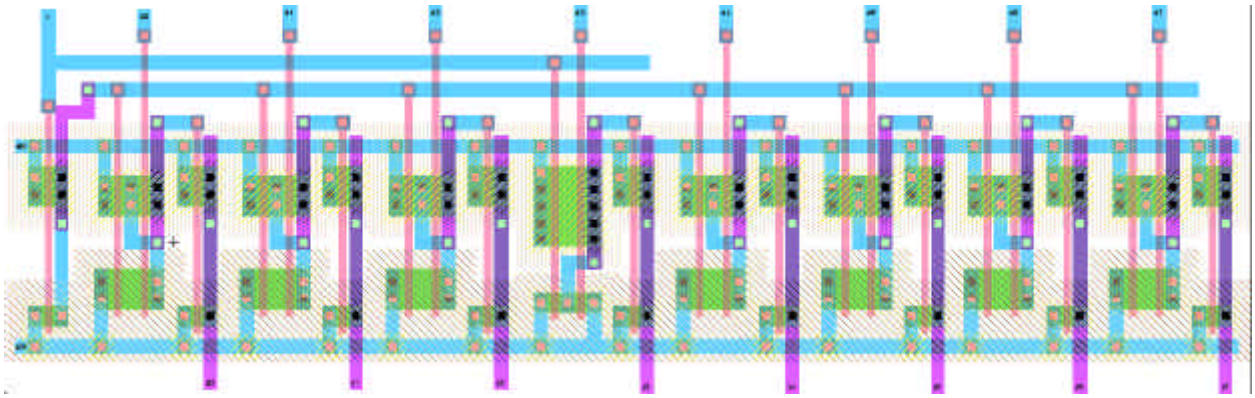
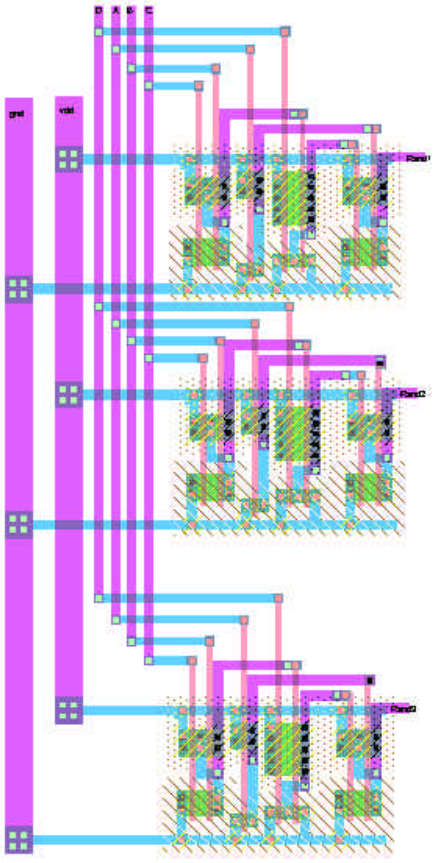


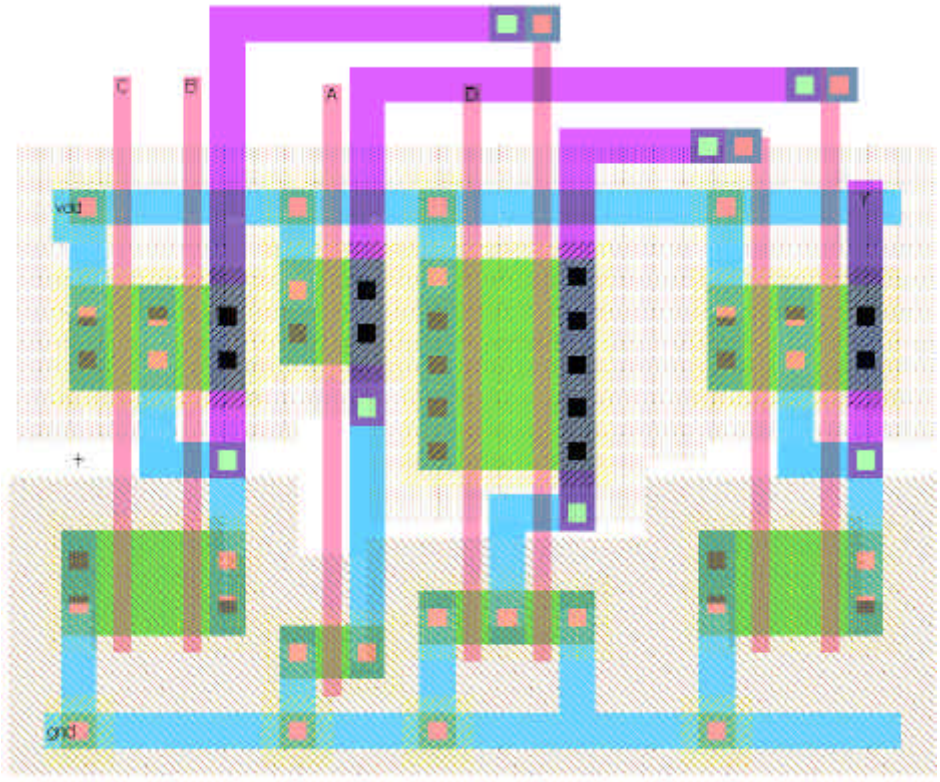
RandomFinal



Random Logic

Amir & Josh

random



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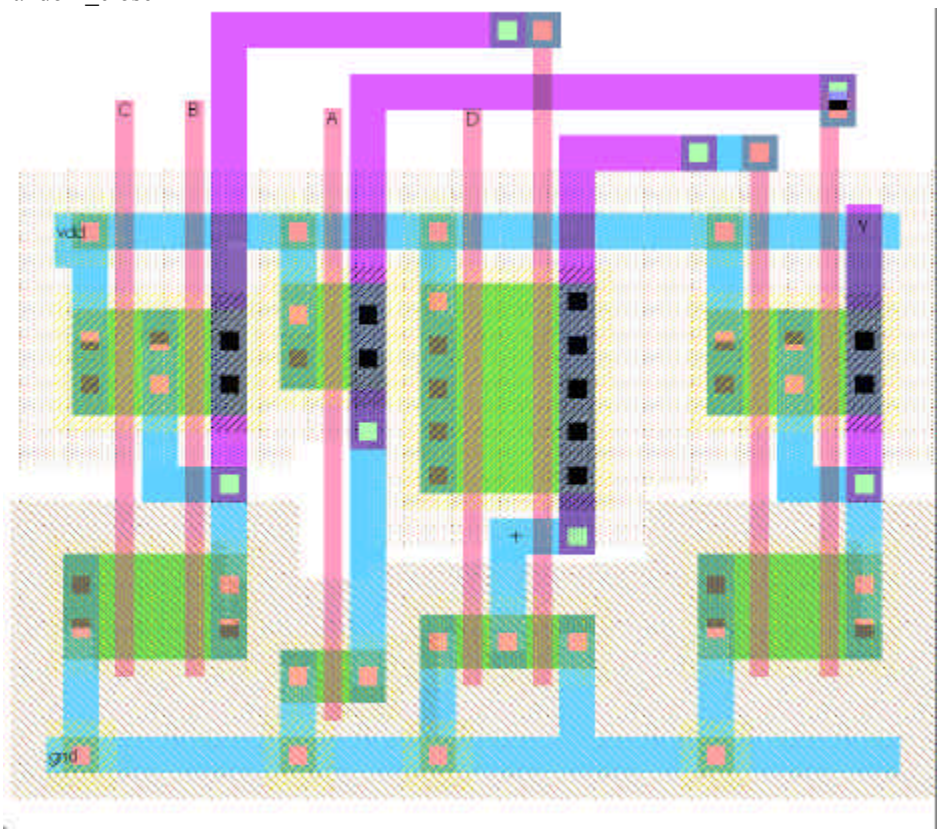

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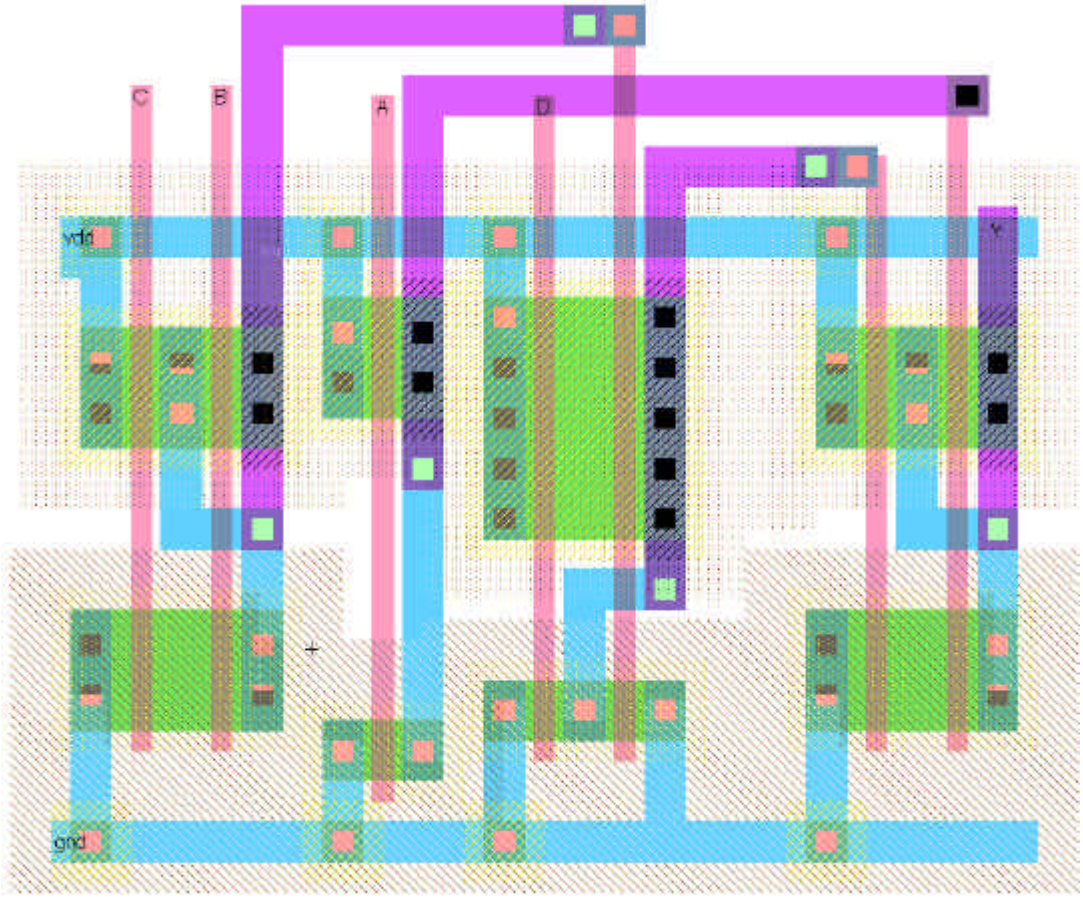
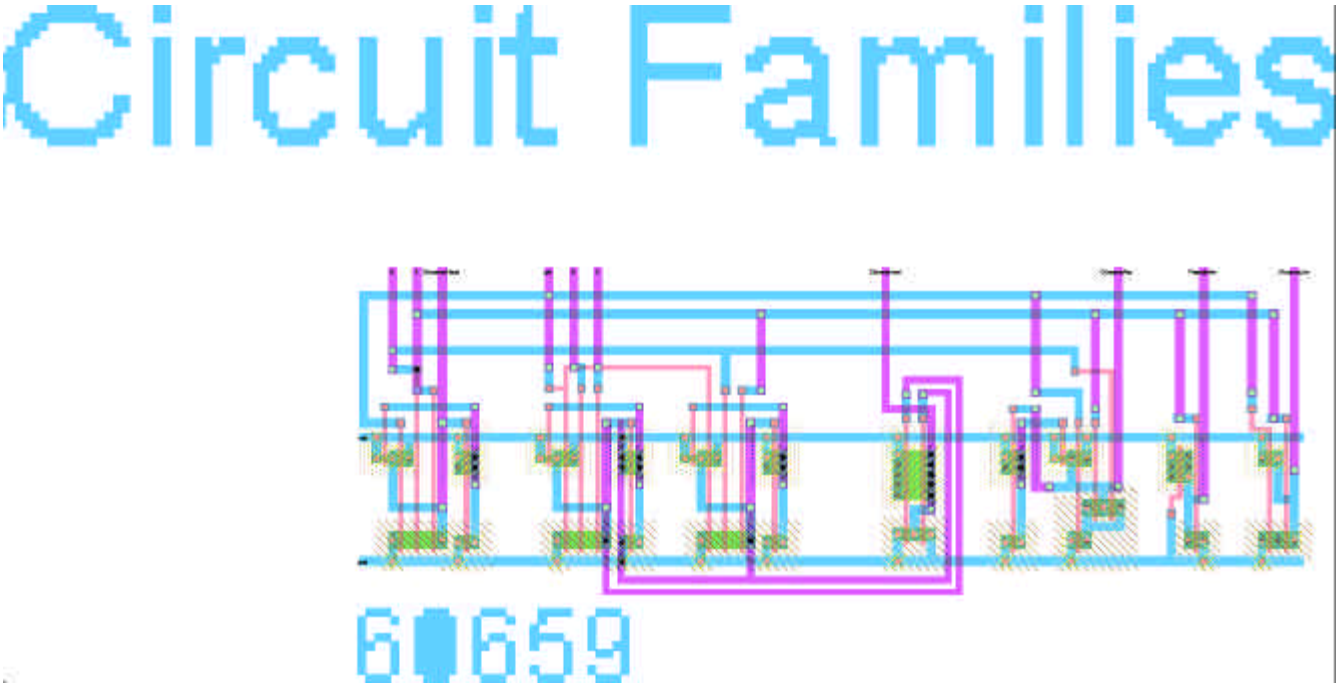
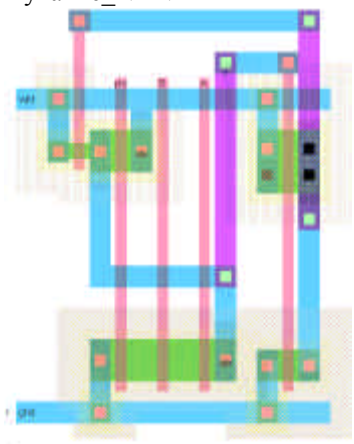


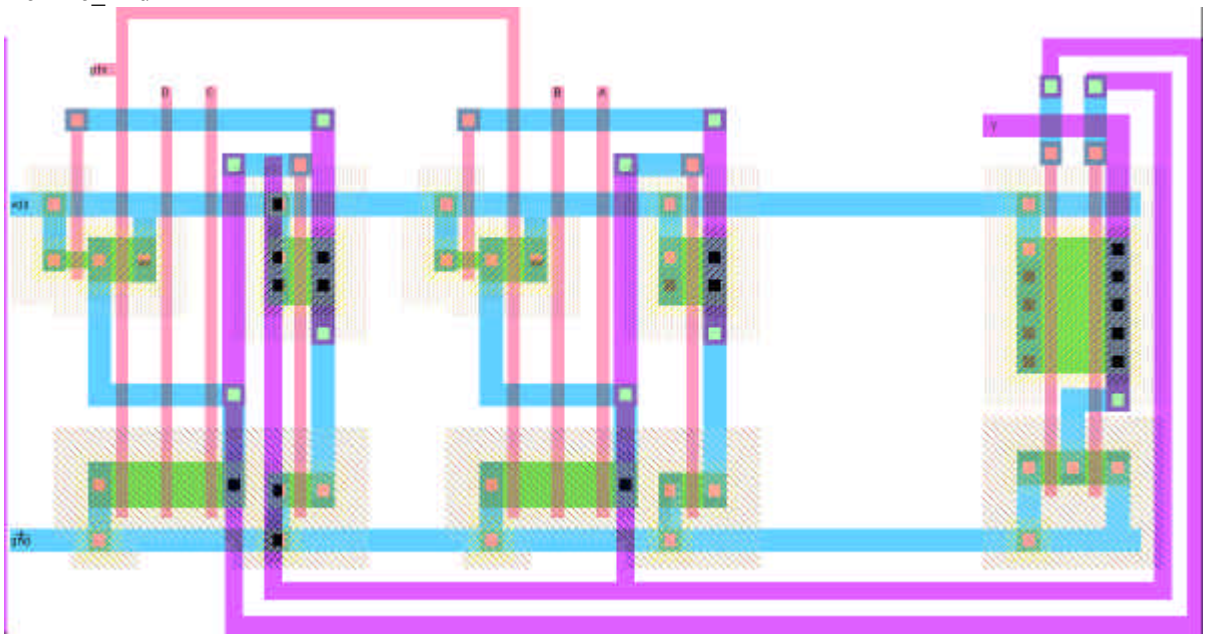
Families



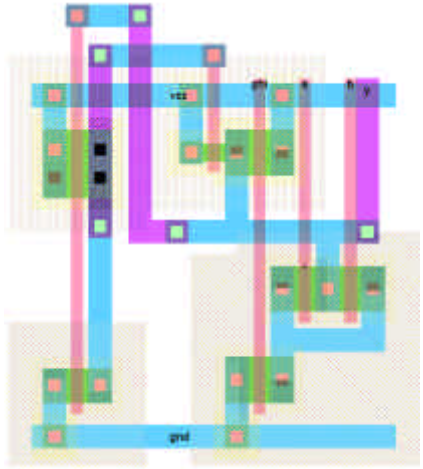
Dynamic_NAND



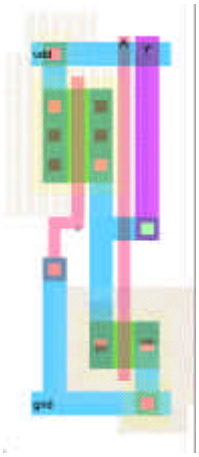
Domino_And



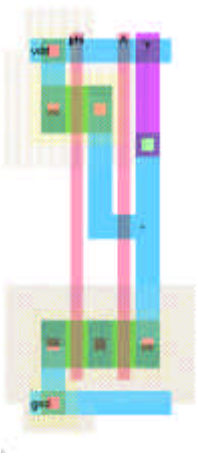
Dynamic_NOR



pseudo_n-MOS



Dynamic_inv



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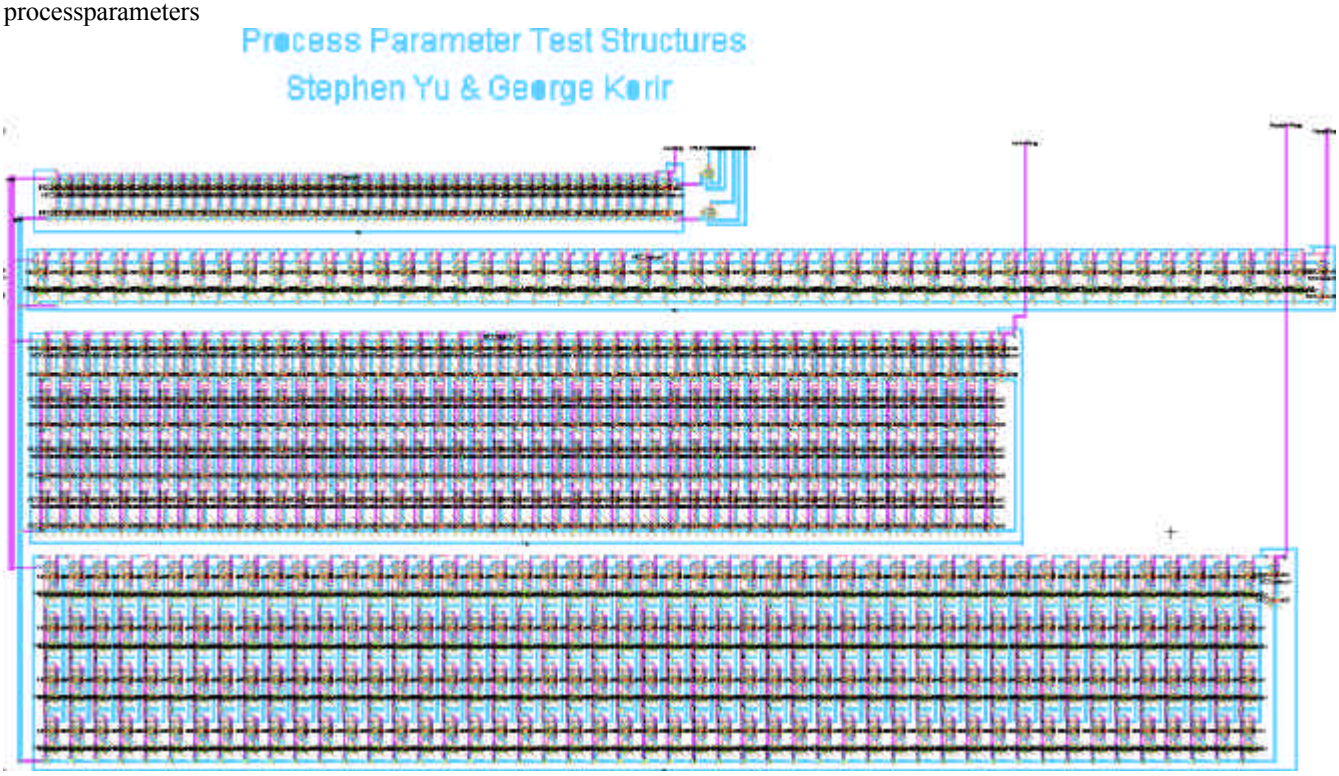

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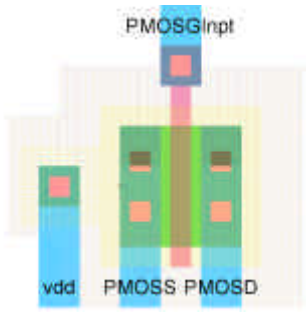

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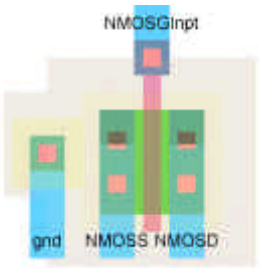

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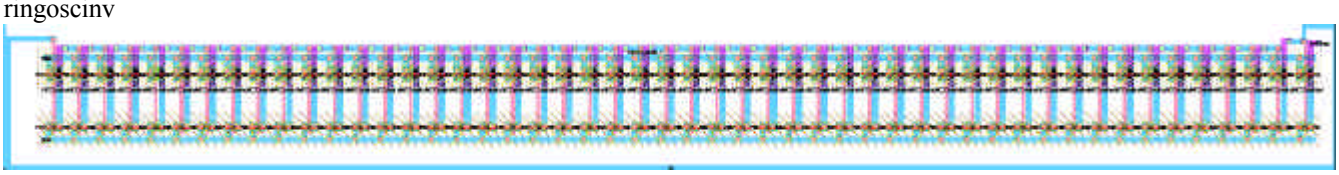
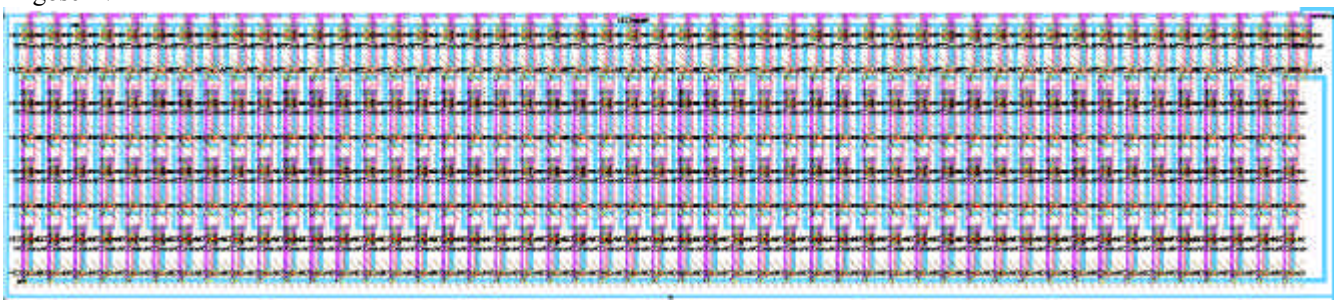


ringoscnand

ringoscinv4



ringoscnand4