17-Jan	Introduction and overview	W 1.1-1.9	
22-Jan	Fabrication and layout	W 3.1-3.7	
24-Jan	Transistor-level implementations		Lab 1 due
29-Jan	Gate design and delay; Switch-level simulation	W 4.2-4.3	PS1 due
31-Jan	Logic optimization		Lab 2 due
5-Feb	-- Intl. Solid State Circuits Conf: No Class --		
7-Feb	Hardware description languages	W 6.1-6.6	Lab 3 due
12-Feb	Clocking	W 5.5	PS2 due
14-Feb	Synthesis and floorplanning		Lab 4 due
19-Feb	Cell design	W 5.1-5.3	
21-Feb	Circuit families	W 5.4	Lab 5 due
26-Feb	Memory design	W 8.3	
28-Feb	Decoders, delay estimation, and gate sizing	W 4.5-4.6	Project proposal due
5-Mar	Logical effort	S Ch. 1-4	PS3 due
7-Mar	Logical effort of circuit families	S Ch. 6-8	
12-Mar	-- Spring Break: No Class --		
14-Mar	-- Spring Break: No Class --		
19-Mar	Adders	W 8.2.1	PS4 due
21-Mar	Datapath functional units	W 8.2	Schematics Complete
26-Mar	Semiconductor economics and scaling	W 4.10-4.13, 6.7	
28-Mar	Design for testability	W 7.1-7.7	
2-Apr	Input / output	W 5.6	PS5 due
4-Apr	Low power design	W 4.7-4.8, 5.7	
9-Apr	Skew-tolerant static circuits	H Ch. 1-2	
11-Apr	Skew-tolerant domino circuits	H Ch. 3-4	Final Project Due
16-Apr	Project Presentations		
18-Apr	Project Presentations		
23-Apr	-- Presentation Days: No Class --		
25-Apr	-- Presentation Days: No Class --		
30-Apr	Trends in VLSI design		PS6 due
2-May	Class summary		